

APPLICATION NOTE

AN1801

10.8MHz FSK decoder with NE564

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FSK DEMODULATION WITH THE 564

The NE564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 1 shows a high-frequency FSK decoder designed for input frequency deviations of +1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from Figure 4a to be approximately 40pF. A trimmer capacitor was added to fine tune f_0' to 10.8MHz.

Figure 2b indicates that the +1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_0' frequencies.

A more thorough analysis confirms these lock range conclusions and serves as a guide for designing other systems. The closed-loop gain of the PLL is equal to the system's lock range and is found as the product of K_d and K_o adjusted to 10.8MHz

$$2\omega_L = K_V = K_d K_o \tag{1}$$

$$2\omega_L = (0.46 \frac{\text{volt}}{\text{radian}}) (0.875 \frac{\text{MHz}}{\text{volt}}) \times (2\pi \times 10.8 \times 10^6 \frac{\text{radian}}{\text{sec}})$$

$$2\omega_L = 2.73 \times 10^7 \frac{\text{radian}}{\text{sec}} \text{ (Lock range total)}$$

Thus Pin 2 could be left as an open circuit and the internally set closed-loop gain would be adequate for tracking the mark and space input frequencies. However, to be safe, a bias adjustment as shown in Figure 1 is recommended to allow for K_d and K_o variations from device to device.

Designing for a capture range of approximately 700kHz gives a low-pass filter time constant of

$$\omega_c \approx \sqrt{\frac{\omega_L}{\tau}} \quad 2\omega_L = K_V = 2.73 \times 10^7 \tag{2}$$

$$(2\pi \times 700 \times 10^3) \approx \sqrt{\frac{2.73 \times 10^7}{\tau}}$$

$$\tau = 1.8\text{ms}$$

Therefore, choose the low-pass filter capacitor as

$$C = \frac{\tau}{R} = \frac{1.41\mu\text{s}}{1.3\text{k}} \approx 1\text{nF} \tag{3}$$

Two 1nF capacitors were selected for the design.

Capacitive coupling was used for the FSK input and is recommended to avoid DC feedthrough. This DC voltage would act

as a DC offset to shift f_0' from 10.8MHz. Balanced biasing with the 1.0kΩ resistors from Pin 7 to Pins 3 and 6 also is recommended to establish symmetrical, quiescent current conditions in the limiter and phase comparator sections of the 564. The 470Ω pull-up resistor for the VCO output was found to give a rise time less than 10ns. This rise time was further reduced by adding the 100Ω resistor between Pins 9 and 11. Figure 3 shows an unmodulated 10.8MHz input signal and the VCO output. Note the approximate 90° phase lag of the VCO output.

A 0.1μF DC retriever capacitor (Pin 14) has less than 1Ω impedance at f_0 , and represents a good compromise between high baud rates (~100k baud) at f_0' and higher-order filtering. If very high baud rates are used, this capacitor could be made smaller with an accompanying increase in the Schmitt trigger hysteresis voltage. The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 5 for 20k, 500k, and 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparator's output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparator's outputs.

The phase comparator's outputs exhibit the waveshapes shown in Figure 4 when the FM input is changed from a square wave FSK modulation to a triangular sweep at a 100Hz modulation rate. The amplitude of the triangular sweep was increased from that used with square wave modulation, causing the loop to be driven in and out of lock. The loop is locked during the smooth, linear portions of the phase comparator's waveshapes and locked during the remaining portions. Lock and capture frequencies were measured for a Pin 2 bias current of 375μA and $f_0' = 10.8\text{MHz}$ as:

$$\text{Lock: } f_{L1} = 6.2\text{MHz} \quad f_{L2} = 16.4\text{MHz}$$

$$\text{Capture: } f_{c1} = 9.3\text{MHz} \quad f_{c2} = 12.2\text{MHz} \quad *P$$

When the loop is locked, the phase detector's outputs represent the demodulated FM output. When unlocked, high frequency harmonics are present, increasing in amplitude until lock is achieved.

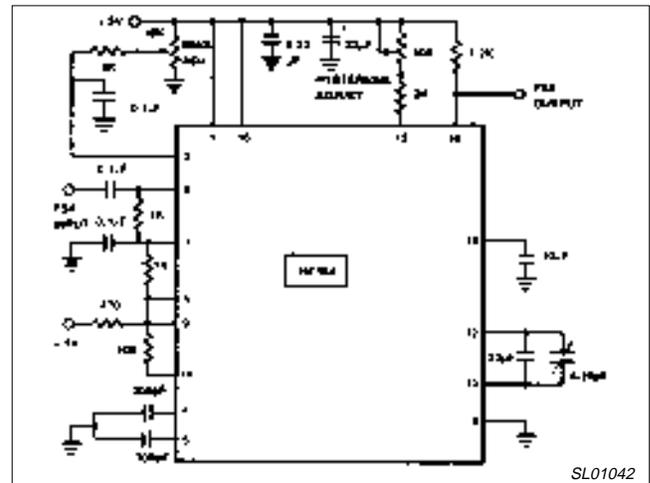


Figure 1. 10.8MHz FSK Decoder Using the NE564

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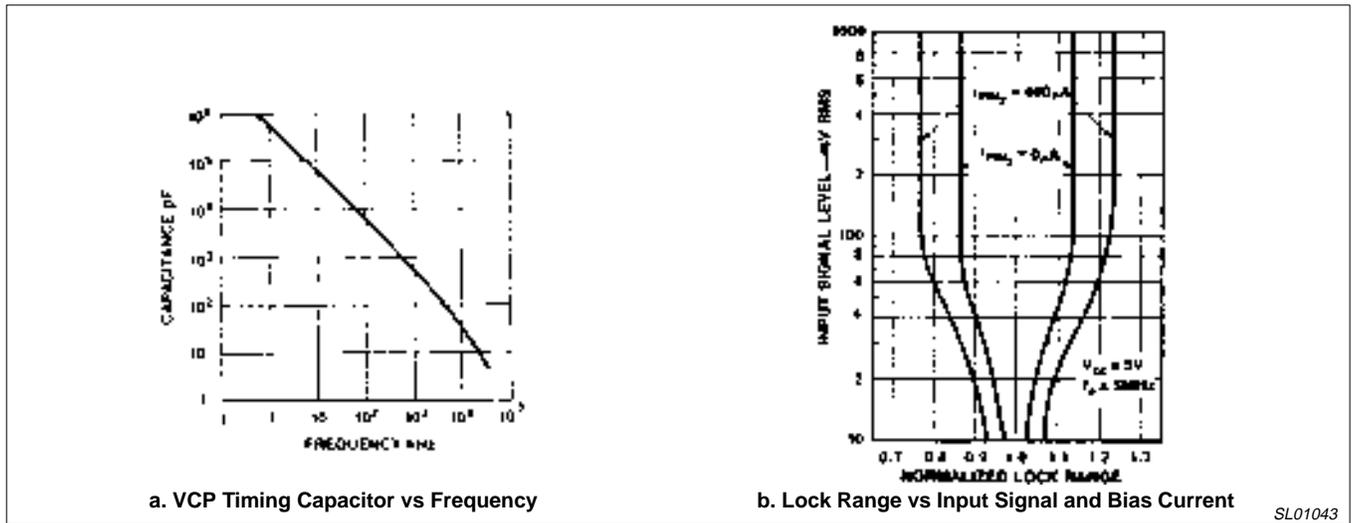


Figure 2. NE564 Characteristics

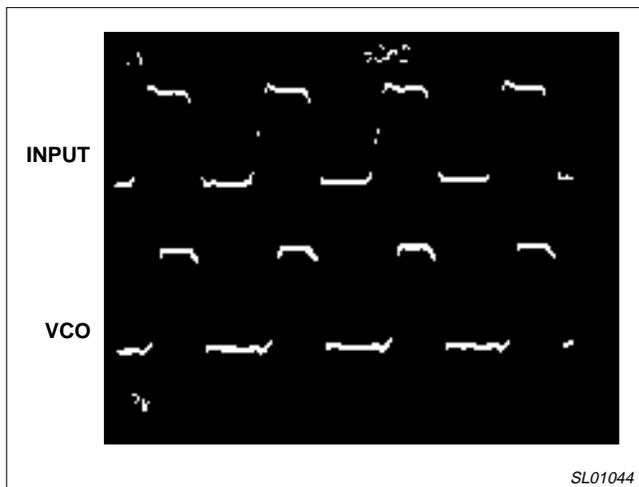


Figure 3. PLL Input and VCO Output for Phase and Frequency Lock at 10.8MHz

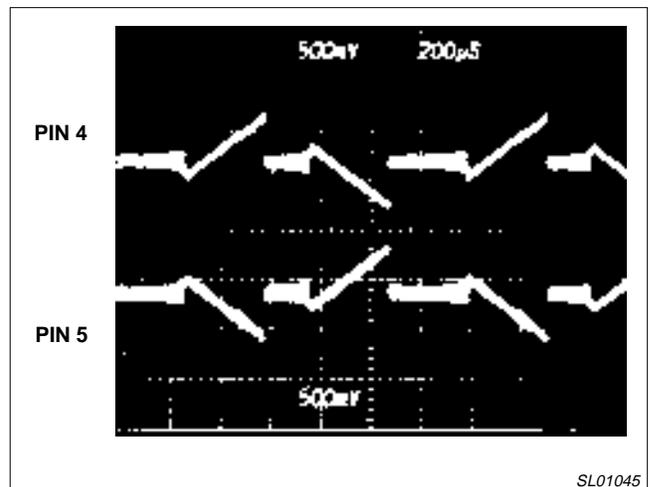


Figure 4. Phase Comparator Outputs Showing Lock and Capture Ranges

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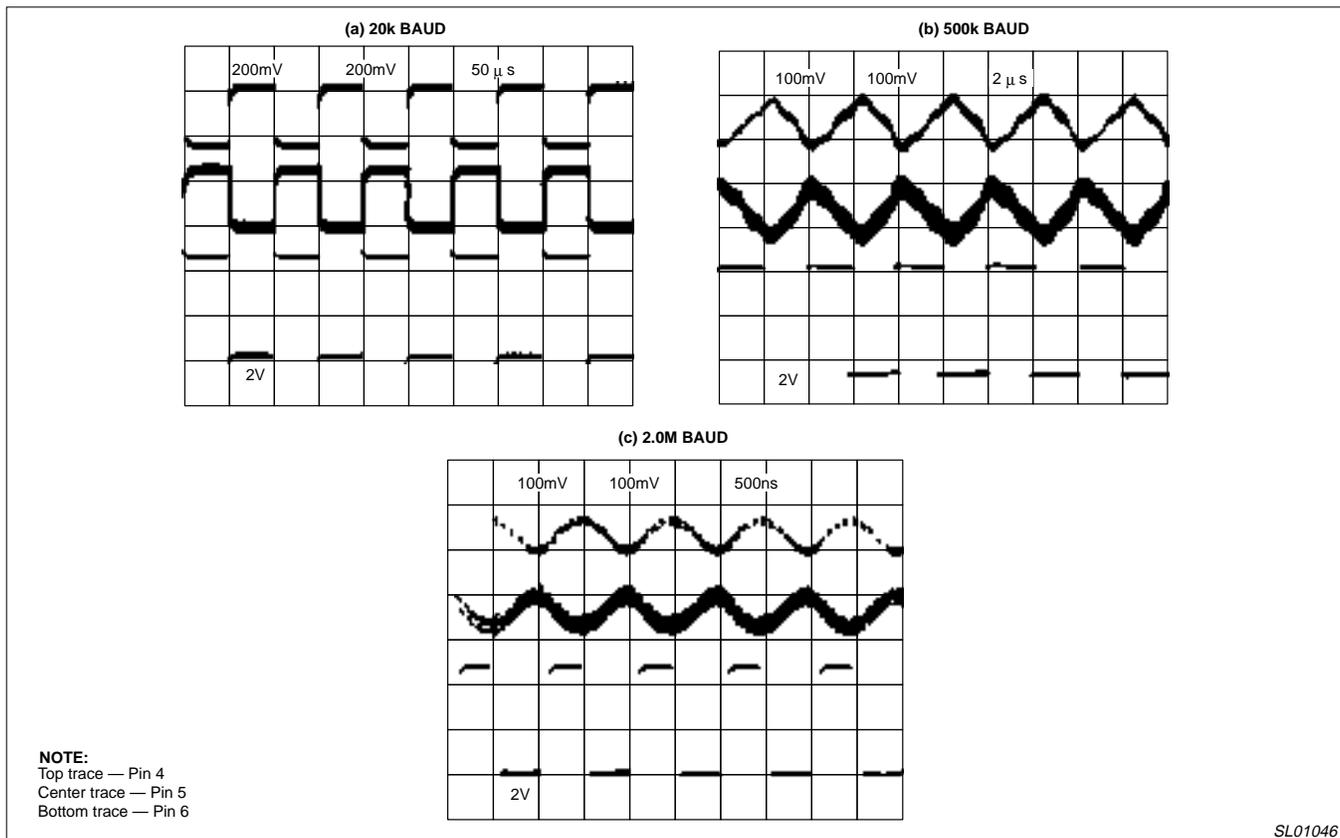


Figure 5. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs for Various Data Rates