

TLC320AD50C ***Data Manual***

Sigma-Delta Analog Interface Circuit
With Master-Slave Function



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1 Introduction

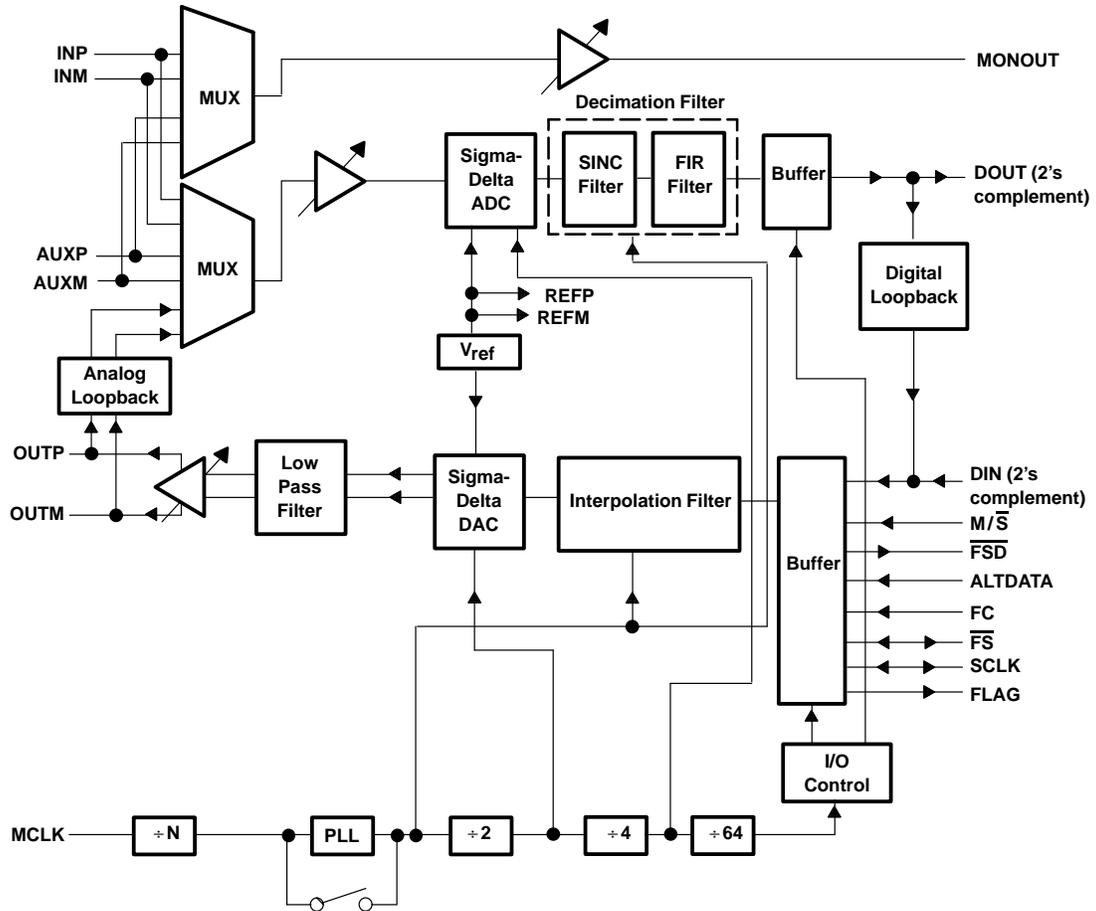
The TLC320AD50C provides high-resolution low-speed signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology. This device consists of two serial synchronous conversion paths (one for each data direction) and includes an interpolation filter before the DAC and a decimation filter after the ADC (see Section 1.2). Other overhead functions provide on-chip timing and control. The sigma-delta architecture produces high-resolution analog-to-digital and digital-to-analog conversion at low system speeds and low cost.

The options and the circuit configurations of this device can be programmed through the serial interface. The options include reset, power down, communications protocol, serial clock rate, signal sampling rate, gain control, and test mode as outlined in Appendix A. The TLC320AD50C is characterized for operation from 0°C to 70°C.

1.1 Features

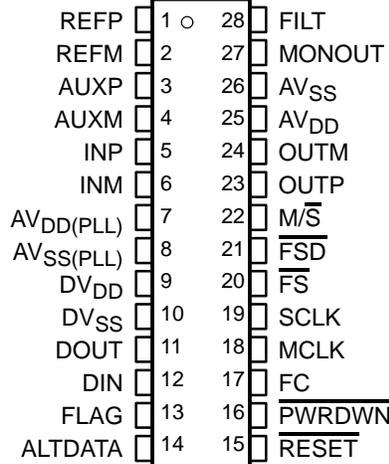
- Single 5-V power supply voltage or 5-V analog and 3-V digital power supply voltages
- Power dissipation (P_D) of 100 mW maximum in the operating mode
- Hardware power-down mode to 2.5 mW
- General-purpose 16-bit signal processing
- 2's-complement data format
- Typical 91-dB dynamic range
- Minimum 88-dB total signal-to-(noise + distortion) for the ADC
- Minimum 85-dB total signal-to-(noise + distortion) for the DAC
- Differential architecture throughout the device
- Internal reference voltage (V_{ref})
- Internal $64 \times$ oversampling for the ADC and $256 \times$ oversampling for the DAC
- Serial port interface
- ALT DATA terminal provides data monitoring during secondary communication
- System test mode, digital loopback test, and analog loopback test
- Supports all V.34 sample rates
- Supports business audio applications
- Variable conversion rate selected as $MCLK/(128 \times N)$ or $MCLK/(512 \times N)$
- May be configured in master or slave mode
- Supports up to three slave devices
- Input and output gain control

1.2 Functional Block Diagram

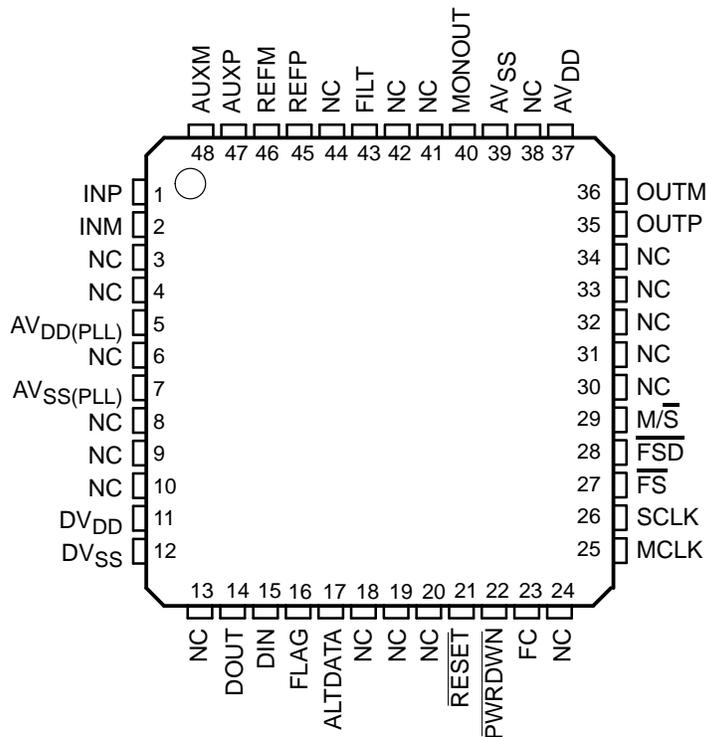


1.3 Terminal Assignments

**DW PACKAGE
(TOP VIEW)**



**PT PACKAGE
(TOP VIEW)**



NC – No internal connection

1.4 Ordering Information

| T _A | PACKAGE | |
|----------------|--------------------------------|---------------------|
| | SMALL OUTLINE PLASTIC DIP (DW) | QUAD FLAT PACK (PT) |
| 0°C to 70°C | TLC320AD50CDW | TLC320AD50CPT |

1.5 Terminal Functions

| TERMINAL | | | I/O | DESCRIPTION |
|------------------------|-----|----|-----|---|
| NAME | NO. | | | |
| | PT | DW | | |
| ALTDATA | 17 | 14 | I | Alternate data. ALTDATA signals are routed to DOUT during secondary communication if ALTDATA is enabled using Control 2 register. |
| AUXM | 48 | 4 | I | Inverting input to auxiliary analog input. AUXM requires an external RC antialias filter. |
| AUXP | 47 | 3 | I | Noninverting input to auxiliary analog input. AUXP requires an external RC antialias filter. |
| AV _{DD} | 37 | 25 | I | Analog ADC path supply (5 V only) |
| AV _{DD} (PLL) | 5 | 7 | I | Analog path supply for the internal PLL (5 V only) |
| AV _{SS} | 39 | 26 | I | Analog ground |
| AV _{SS} (PLL) | 7 | 8 | I | Analog ground for the internal PLL |
| DIN | 15 | 12 | I | Data input. DIN receives the DAC input data and command information from the digital signal processor and is synchronized to SCLK. |
| DOUT | 14 | 11 | O | Data output. DOUT transmits the ADC output bits and is synchronized to SCLK. DOUT is at high impedance when FS is not activated. |
| DV _{DD} | 11 | 9 | I | Digital power supply (5 V or 3 V) |
| DV _{SS} | 12 | 10 | I | Digital ground |
| FC | 23 | 17 | I | Function code. FC is sampled and latched on the rising edge of \overline{FS} for the primary serial communication. If slave devices are present, the FC terminal of all devices should be tied together. See Section 3, <i>Serial Communications</i> for more details. |
| FILT | 43 | 28 | O | Bandgap filter. FILT is provided for decoupling of the bandgap reference, and provides 3.2 V. The optimal capacitor value is 0.1 μ F (ceramic). This voltage node should be loaded only with a high-impedance dc load. |
| FLAG | 16 | 13 | O | Output flag. During phone mode, FLAG contains the value set in Control 2 register. |
| \overline{FS} | 27 | 20 | I/O | Frame sync. When \overline{FS} goes low, DIN begins receiving data bits and DOUT begins transmitting data bits. In master mode, \overline{FS} is low during the simultaneous 16-bit transmission to DIN and from DOUT. In slave mode, \overline{FS} is externally generated and must be low for one SCLK period minimum to initiate the transfer. |
| \overline{FSD} | 28 | 21 | O | Frame sync delayed output. The \overline{FSD} (active-low) output synchronizes a slave device to the frame sync of the master device. \overline{FSD} is applied to the slave \overline{FS} input and is the same duration as the master \overline{FS} signal but delayed in time by the number of shift clocks programmed in the \overline{FSD} register. |
| INM | 2 | 6 | I | Inverting input to analog modulator. INM requires an external RC antialias filter. |
| INP | 1 | 5 | I | Noninverting input to analog modulator. INP requires an external RC antialias filter. |

NOTE 1: All digital inputs and outputs are TTL compatible, unless otherwise noted (for DV_{DD} = 5 V).

1.5 Terminal Functions (Continued)

| TERMINAL | | | I/O | DESCRIPTION |
|---------------------------|-----|----|-----|--|
| NAME | NO. | | | |
| | PT | DW | | |
| $\overline{M/S}$ | 29 | 22 | I | Master/slave select input. When $\overline{M/S}$ is high, the device is the master, and when low it is a slave. |
| MCLK | 25 | 18 | I | Master clock. MCLK derives the internal clocks of the sigma-delta analog interface circuit. |
| MONOUT | 40 | 27 | O | Monitor output. MONOUT allows for monitoring of the analog input and is a high-impedance output. The gain or mute is selected using control register 2. |
| OUTM | 36 | 24 | O | Inverting output of the DAC. The OUTM output can be loaded with 600 Ω differentially or single-ended. OUTM is functionally identical with and complementary to OUTP. OUTM can also be used alone for single-ended operation. |
| OUTP | 35 | 23 | O | Noninverting output of the DAC. The OUTP output can be loaded with 600 Ω differentially or single-ended. OUTP can also be used alone for single-ended operation. |
| \overline{PWRDWN} | 22 | 16 | I | Power down. When \overline{PWRDWN} is pulled low, the device goes into a power-down mode, the serial interface is disabled, and most of the high-speed clocks are disabled. However, all the register values are sustained and the device resumes full power operation without reinitialization when \overline{PWRDWN} is pulled high again. \overline{PWRDWN} resets the counters only and preserves the programmed register contents (see Subsection 3.3.3). |
| REFM | 46 | 2 | O | Voltage reference filter input. REFM is provided for low-pass filtering of the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF to REFP. DC voltage at REFM is 0 V. |
| REFP | 45 | 1 | O | Voltage reference filter positive input. REFP is provided for low-pass filtering of the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF to REFM. DC voltage at REFP is 3.2 V. REFP should be loaded only with a high-impedance dc load. |
| $\overline{\text{RESET}}$ | 21 | 15 | I | Reset. The reset function is provided to initialize all of the internal registers to their default values. The serial port can be configured to the default state accordingly. See Appendix A, <i>Register Set Control 1</i> register and Subsection 2.2.1, <i>Reset and Power-Down Functions</i> for more detailed descriptions. |
| SCLK | 26 | 19 | I/O | Shift clock. SCLK signal clocks serial data into DIN and out of DOUT during the frame-sync interval. When configured as an output ($\overline{M/S}$ high), SCLK is generated internally by multiplying the frame-sync signal frequency by 256. When configured as an input ($\overline{M/S}$ low), SCLK is generated externally and must be synchronous with the master clock and frame sync. |

NOTE 1: All digital inputs and outputs are TTL compatible, unless otherwise noted (for $\text{DV}_{\text{DD}} = 5 \text{ V}$).

1.6 Definitions and Terminology

| | |
|--------------------------------|--|
| Data Transfer Interval | The data transfer interval is the time during which data is transferred from DOUT and to DIN. The interval is 16 shift clocks and the data transfer is initiated by the falling edge of the frame-sync signal. |
| Signal Data | Signal data refers to the input signal and all of the converted representations through the ADC channel and returned through the DAC channel to the analog output. This is contrasted with the purely digital software control data. |
| Primary Communications | Primary communications refers to the digital data transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously. |
| Secondary Communications | Secondary communications refers to the digital control and configuration data transfer interval into DIN and the register read data cycle from DOUT. The data transfer interval occurs when requested by hardware or software. |
| Frame Sync | Frame sync refers only to the falling edge of the signal that initiates the data transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications. |
| Frame Sync and Sampling Period | Frame sync and sampling period is the time between falling edges of successive primary frame-sync signals. |
| f_s | The sampling frequency that is the reciprocal of the sampling period. |
| Frame-Sync Interval | Frame-sync interval is the the time period occupied by 256 shift clocks. The frame-sync signal goes high on the sixteenth rising edge of SCLK after the falling edge of the frame-sync signal. |
| ADC Channel | ADC channel refers to all signal processing circuits between the analog input and the digital conversion results at DOUT. |
| DAC Channel | DAC channel refers to all signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUP and OUTM. |
| Host | A host is any processing system that interfaces to DIN, DOUT, SCLK, or \overline{FS} . |
| Dxx | Dxx is the bit position in the primary data word (xx is the bit number). |
| DSxx | DSxx is the bit position in the secondary data word (xx is the bit number). |
| d | The alpha character d represents valid programmed or default data in the control register format (see Section 3.2, <i>Secondary Serial Communication</i>) when discussing other data bit portions of the register. |
| X | The alpha character X represents a don't care bit position within the control register format. |
| FIR | Finite duration impulse response |

1.7 Register Functional Summary

There are seven data and control registers that are used as follows:

- Register 0 The No-Op register. The 0 address allows secondary requests without altering any other register.
- Register 1 The Control 1 register. The data in this register controls:
- The software reset
 - The software power down
 - Normal or auxiliary analog inputs enabling
 - Selection of the digital loopback
 - 16-bit or 15-bit mode of operation
 - Selection of monitor amplifier output gain
 - Selection of hardware or software secondary request mode
- Register 2 The Control 2 register. The data in this register:
- Contains the output flag indicating a decimator FIR filter overflow
 - Contains the output value of FLAG
 - Enables the ALTDATA input
 - Selects either 16-bit mode or 15-bit mode for the ADC
 - Enables analog loopback
- Register 3 The Control 3 register. The data in this register:
- Selects the number of SCLK delays between \overline{FS} and \overline{FSD}
 - Informs the master device of how many slaves are connected in the chain.
- Register 4 The Control 4 register. The data in this register:
- Selects the amplifier gain for the input and output amplifiers
 - Sets the sample rate by choosing the value of N from 1 to 8 where $f_s = MCLK/(128 \times N)$ or $MCLK/(512 \times N)$
 - Enables the external sample clock input at the MCLK input and bypasses the internal PLL. When enabled, the sample rate is set to $MCLK/(512 \times N)$ (see Subsection 2.1.1, *Operating Frequencies* for more details.
- Register 14 Reserved for factory test. Do not write to this register.
- Register 15 Reserved for factory test. Do not write to this register.

2 Functional Description

2.1 Device Functions

2.1.1 Operating Frequencies

The sampling (conversion) frequency is derived from the master clock (MCLK) input by equation 1.

$$f_s = \text{Sampling (conversion) frequency} = \frac{\text{MCLK}}{128 \times N} \quad (\text{when bit D7 of register 4 is set to 0}) \quad (1)$$

where N is set by the contents of register 4 (bits D4 – D6). The value of N must be from 1 to 8. If the value of register 4 (bits D4 – D6) is 000, it defaults to N = 8. Otherwise, N is set by the octal representation of register 4 (bits D4 – D6). This is valid for sample rates higher than 7 kHz.

For sample rates lower than 7 kHz, the external sample clock feature must be enabled. This is done by setting bit D7 of Control 4 register equal to 1. This then bypasses the internal clock phase lock loop (PLL) and sets the sampling frequency according to equation 2.

$$f_s = \frac{\text{MCLK}}{512 \times N} \quad (\text{when bit D7 of register 4 is set to 1}) \quad (2)$$

This feature can be enabled for any sample rate, but must be enabled for sample rates lower than 7 kHz. The default value for register 4 bit D7 is 1. In all cases where the external sample clock is not used, 200 μs must be allowed following a change in the value of N for the PLL to settle. During this period, there is no signal output on the frame-sync or shift clock terminals.

The inverse of the sample frequency is the time between the falling edges of two successive primary frame-sync signals which is the conversion period.

2.1.2 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data.

The input signal is filtered and applied to the ADC input. The ADC converts the signal into discrete output digital words in 2's-complement data format, corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port (DOUT) during the frame-sync interval, one word for each primary communication interval. During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address, and the read bit set to 1. If a register read is not requested, all 16 bits are cleared to 0 in the secondary word.

2.1.3 DAC Signal Channel

DIN receives the 16-bit serial data word (2's complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to a pulse train by the sigma-delta DAC comprised of a digital interpolation filter and a digital 1-bit modulator. The output of the modulator is then passed to an internal low-pass filter to complete the signal reconstruction resulting in an analog signal.

2.1.4 Serial Interface

The digital serial interface consists of the shift clock, the frame-sync signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame synchronization interval, SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-sync interval, SCLK transfers the register read data from DOUT if the read bit is set to 1. In addition, SCLK transfers control and device parameter information into DIN. The timing sequence is shown in Figure 3–1.

2.1.5 Register Programming

All register programming occurs during secondary communications, and data are latched and valid on the rising edge of the frame-sync signal. If the default value for a particular register is desired, that register does not need to be addressed during the secondary communications. The no-op command addresses the pseudo-register (register 0), and no register programming takes place during the communications.

DOOUT is released from the high-impedance state on the falling edge of the primary or secondary frame-sync interval. In addition, each register can be read back during DOOUT secondary communications by setting the read bit D13 to 1. When the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication.

2.1.6 Sigma-Delta ADC

The sigma-delta ADC is a fourth-order sigma-delta modulator with $64\times$ oversampling. The ADC provides high-resolution, low-noise performance using oversampling techniques.

2.1.7 Decimation Filter

The decimation filter reduces the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:64. The output of the decimation filter is a 16-bit 2's-complement data word clocking at the sample rate selected.

NOTE:

The sample rate is determined through a relationship of $MCLK/(128 \times N)$ where N is set by bits D4 – D6 of register 4 when bit D7 of register 4 is cleared to 0. The relationship when bit D7 of register 4 is set to 1 is $MCLK/(512 \times N)$.

2.1.8 Sigma-Delta DAC

The sigma-delta DAC is a second-order sigma-delta modulator with 256 times oversampling. The DAC provides high-resolution, low-noise performance from a 1-bit converter using oversampling techniques. The TLC320AD50C provides a voltage output DAC.

2.1.9 Interpolation Filter

The interpolation filter resamples the digital data at a rate of $256\times$ the incoming sample rate. The high-speed data output from the interpolation filter is then used in the sigma-delta DAC.

2.1.10 Analog and Digital Loopback

The loopbacks provide a means of testing the ADC and DAC channels and can be used for in-circuit system-level tests. The loopbacks feed the appropriate output to the corresponding input on the IC.

The test capabilities include an analog loopback between the two analog paths and a digital loopback between the two digital paths. Digital loopback is enabled by setting bit D1 in Control 1 register. Analog loopback is enabled by setting bit D3 in Control 2 register (see Appendix A, *Register Set*).

2.1.11 FIR Overflow Flag

The decimator FIR filter provides an overflow flag to Control 2 register to indicate that the input to the filter has exceeded the range of the internal filter calculations. When the FIR overflow flag (Control 2 register bit D5) is set in the register, it remains set until the register is read by the user. Reading this value always resets the overflow flag.

2.2 Terminal Functions

2.2.1 Reset and Power-Down Functions

2.2.1.1 Reset

The TLC320AD50C resets both the internal counters and registers, including the programmed registers, in two ways:

1. By applying a low-going reset pulse to the reset terminal
2. By writing to the programmable software reset bit (D7 in Control 1 register)

$\overline{\text{PWRDWN}}$ resets the counters only and preserves the programmed register contents. The $\overline{\text{PWRDWN}}$ terminal must be kept low 20 ms after the power supplies have settled.

2.2.1.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are:

1. Counter reset – The counter reset signal resets all flip-flops and latches that are not externally programmed, with the exception of those generating the reset pulse itself. Additionally, this signal resets the software power-down bit. A counter reset is initiated with the $\overline{\text{RESET}}$ terminal or RESET bit or $\overline{\text{PWRDWN}}$ terminal.
2. Register reset – The register reset signal resets all flip-flops and latches that are not reset by the counter reset, except those generating the reset pulse itself. A register reset is initiated with the $\overline{\text{RESET}}$ terminal or RESET bit.

Both reset signals must be at least six master clock periods long, T_{RESET} , and releases on the trailing edge of the master clock.

2.2.1.3 Software and Hardware Power Down

Given the definitions above, the software-programmed power-down condition is cleared by programming the software bit (Control 1 register, bit 6) to 0 or by cycling the power to the device or bringing $\overline{\text{RESET}}$ low.

The output of the monitor amplifier maintains its midpoint voltage during hardware and software power down to minimize pops and clicks.

$\overline{\text{PWRDWN}}$ powers down the entire chip. Cycling the power-down terminal from high to low and back to high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents.

If $\overline{\text{PWRDWN}}$ is not used, it should be tied high. The power drawn during a software power down is higher than during a hardware power down. This is due to the current drawn to keep the digital interface running.

2.2.2 Master Clock Circuit

The clock circuit generates and distributes necessary clocks throughout the device. MCLK is the external master clock input. An internal PLL circuit is used for upsampling to provide the appropriate clocks for the digital filters and modulators. When in master mode, SCLK is derived from MCLK in order to provide clocking of the serial communications between the device and a digital signal processor. When in slave mode, SCLK and MCLK are both inputs. The sample rate of the data paths is set as $\text{MCLK}/(128 \times N)$ where N is set by the contents of bits D4 – D6 of Control 4 register when bit D7 of Control 4 register is cleared to 0. This is only valid for sample rates greater than 7 kHz.

For sample rates lower than 7 kHz, the internal PLL must be bypassed by enabling the external sample clock feature (setting bit D7 of Control 4 register to 1. This changes the relationship between the master clock frequency and the sample rate. When this feature is enabled, the sample rate of the data paths is set as $\text{MCLK}/(512 \times N)$. This feature can be enabled for sample rates higher than 7 kHz.

2.2.3 Data Out (DOUT)

DOUT is placed in the high-impedance state on the sixteenth rising edge of SCLK (internal or external) after the falling edge of the frame sync. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write (R/W) bit with the eight MSBs set to 0 (see Section 3, *Serial Communications*). If a register read is not requested, the secondary word is all zeroes. The state of the master/slave terminal is reflected by the MSB in secondary communication and the LSB in the primary communication. When the device is in the slave mode, DOUT remains as 3-state during initialization until a nonzero value is written to Control 3 register (bits D7 and D6).

2.2.3.1 Data Out, Master Mode

In the master mode, DOUT is taken from the high-impedance state by the falling edge of the frame sync. The most significant data bit then appears on DOUT.

2.2.3.2 Data Out, Slave Mode

In the slave mode, DOUT is taken from the high-impedance state by the falling edge of the external frame sync. The most significant data bit then appears on DOUT. When in slave mode, DOUT is not enabled until Control 3 register is programmed with the number of slaves. This must be done even if there is only one slave device.

2.2.4 Data In (DIN)

In a primary communication, the data word is the input digital signal to the DAC channel. In a secondary communication, the data is the control and configuration data sets the device for a particular function (see Section 3, *Serial Communications*). The LSB of Control 1 register determines whether the input is 15 bits or 16 bits.

2.2.5 FC (Hardware Program Terminal)

The FC input provides for hardware programming requests for secondary communication. FC works in conjunction with the control bit D0 of the secondary data word. The signal on FC is latched on the rising edge of the primary frame sync. See Figure 5–4 for the FC timing diagrams. FC should be tied low if not used (see Section 3.2, *Secondary Serial Communication* and Table 3–2).

2.2.6 Frame-Sync Function

The frame-sync signal indicates the device is ready to send and receive data. The data transfer from DOUT and into DIN begins on the falling edge of the frame-sync signal.

2.2.6.1 Frame Sync (\overline{FS}), Master Mode

The frame sync is generated internally and goes low on the rising edge of SCLK and remains low during a 16-bit data transfer. In addition to generating its own frame-sync signal, the master also outputs a frame sync for each slave that is being used.

2.2.6.2 Frame Sync, (\overline{FS}) Slave Mode

The frame-sync timing is generated externally by the master, is applied to \overline{FS} of the slave, and controls the ADC and DAC timing in the case of a single slave. The external frame-sync width must be a minimum of one shift clock to be recognized and can be as long as 16 shift clocks.

2.2.6.3 Frame-Sync Delayed ($\overline{\text{FSD}}$), Master Mode

For the master, the frame-sync delayed output occurs 1/2 shift-clock period ahead of $\overline{\text{FS}}$ to compensate for the time delay through the master and slave devices. The timing relationships are as follows:

1. When the FSD register data is 0, then $\overline{\text{FSD}}$ goes low 1/4 SCLK prior to the rising edge of SCLK when $\overline{\text{FS}}$ goes low (see Figure 5–1).
2. When the FSD register data is greater than 17, then $\overline{\text{FSD}}$ goes low on the rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{\text{FS}}$.

Register data values from 1 to 17 result in a default register value of zero and should not be used.

In either master or slave mode, if the number of slave devices (bits D0 and D1 of Control 2 register) is set to 0, then FSD is disabled.

2.2.6.4 Frame-Sync Delayed ($\overline{\text{FSD}}$), Slave Mode

The master $\overline{\text{FSD}}$ is output to the first slave and the first slave $\overline{\text{FSD}}$ is output to the second slave device and so on. The $\overline{\text{FSD}}$ output of each device is input to the $\overline{\text{FS}}$ terminal of the succeeding device. The FSD timing sequence in the slave mode is as follows:

1. When the FSD register data is 0, then $\overline{\text{FSD}}$ goes low after $\overline{\text{FS}}$ goes low (see Figure 5–2).
2. When the FSD register data is greater than 17, $\overline{\text{FSD}}$ goes low on the rising edge of SCLK that is the FSD register number of SCLKs after the falling edge of $\overline{\text{FS}}$.

Data values from 1 to 17 should not be used.

2.2.7 Multiplexed Analog Input

The two differential analog inputs (INP and INM or AUXP and AUXM) are multiplexed into the sigma-delta modulator. The performance of the AUX channel is similar to the normal input channel. A simple RC antialias filter must be connected to AUXP and AUXM (also INP and INM if used). Amplifiers are provided to set the gain of each input. The gain of these amplifiers is set by the contents of control 4 register (see Appendix A, *Register Set* for details).

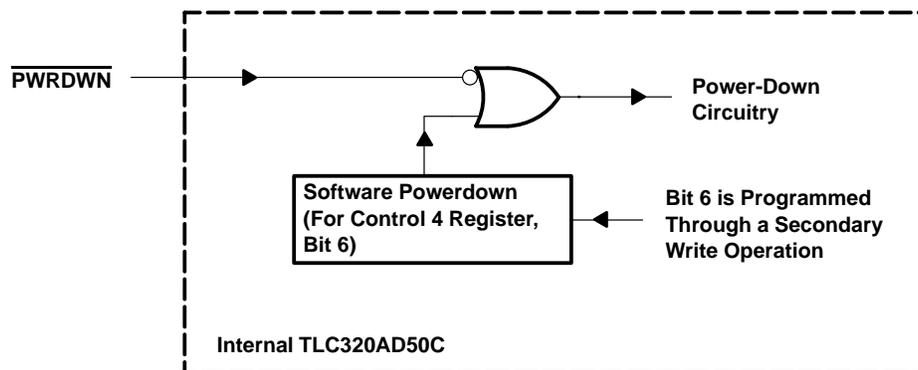


Figure 2–1. Internal Power-Down Logic

2.2.8 Analog Input

The signal applied to the terminals INM and INP shown in Figure 2–2 should be differential to preserve the device specifications. A single-ended input signal should always be converted to a differential input signal prior to being used by the TLC320AD50C. The signal source driving the analog inputs (INM, INP, AUXM, AUXP) should have a low source impedance for lowest noise performance and accuracy. To obtain maximum dynamic range, the input signal should be centered at midsupply. The analog input signal is self-biased to the mid-supply voltage if the monitor-amplifier input source is selected as the same source for the ADC input. These input sources are selected by bits D4 and D5 of Control 1 register. The default condition self biases the input since the register default value selects INP and INM as the source for both the ADC and monitor amplifier inputs. A simple RC antialias filter must be connected to INP and INM (also AUXP and AUXM if used).

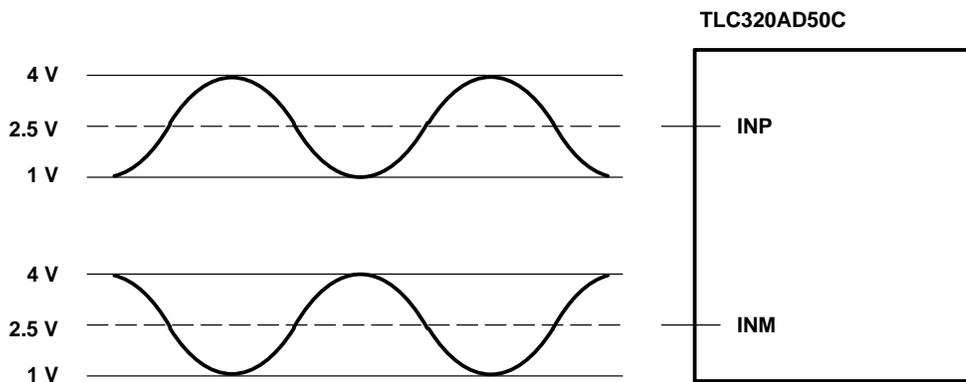


Figure 2–2. Differential Analog Input Configuration

3 Serial Communications

DOUT, DIN, SCLK, \overline{FS} , and FC are the serial communication signals. The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronizing clock for the serial communication data and the frame sync is taken from SCLK. The frame-sync pulse that encloses the ADC and DAC data transfer interval is taken from \overline{FS} . For signal (audio) data transmitted from the ADC or to the DAC, primary serial communication is used. To read or write words that control both the options and the circuit configurations of the device, secondary communication is used.

The purpose of the primary and secondary communications is to allow conversion data and control data to be transferred across the same serial port. A primary transfer is always dedicated to conversion data. A secondary transfer is used to set up and read the register values described in Appendix A, *Register Set*. A primary transfer occurs for every conversion period. A secondary transfer occurs only when requested. Two methods exist for requesting a secondary command. The FC terminal can request a secondary communication when it is asserted, or the LSB of the DAC data within a primary transfer can request a secondary communication. The selection of which method is enabled is provided in Control 1 register (bit D0) as shown in Appendix A, *Register Set*.

For all serial communications, the most significant bit is transferred first. For a 16-bit ADC word and a 16-bit DAC word, D15 is the most significant bit and D0 is the least significant bit. For a 15-bit DAC data word in a 16-bit primary communication, D15 is the most significant bit, D1 is the least significant bit, and D0 is used for the embedded function control. All digital data values are in 2's-complement data format.

These logic signals are compatible with TTL-voltage levels and CMOS current levels (when $V_{DD} = 5$ Vdc). These logic signals are also compatible with a 3-V supply.

3.1 Primary Serial Communication

Primary serial communication is used both to transmit and receive conversion signal data. The ADC word length can be either 15 bits or 16 bits. In master mode with \overline{FSD} disabled, it is always 16 bits. In slave mode, it is always 15 bits. The DAC word length depends on the status of D0 in Control 1 register. After power up or reset, the device defaults to 15-bit mode (not 16-bit mode). The DAC word length is 15 bits and the last bit of the primary 16-bit serial communication word is a function control bit used to request secondary serial communication. In 16-bit mode, all 16 bits of the primary communication word are used as data for the DAC and the hardware terminal FC must be used to request secondary communication.

Figure 3–1 shows the timing relationship for SCLK, \overline{FS} , DOUT and DIN in a primary communication. The timing sequence for this operation is as follows:

1. \overline{FS} is brought low by the TLC320AD50C.
2. One 16-bit word is transmitted from the ADC (DOUT) and one 16-bit word is received for the DAC (DIN).
3. \overline{FS} is brought high by the TLC320AD50C signaling the end of conversion.

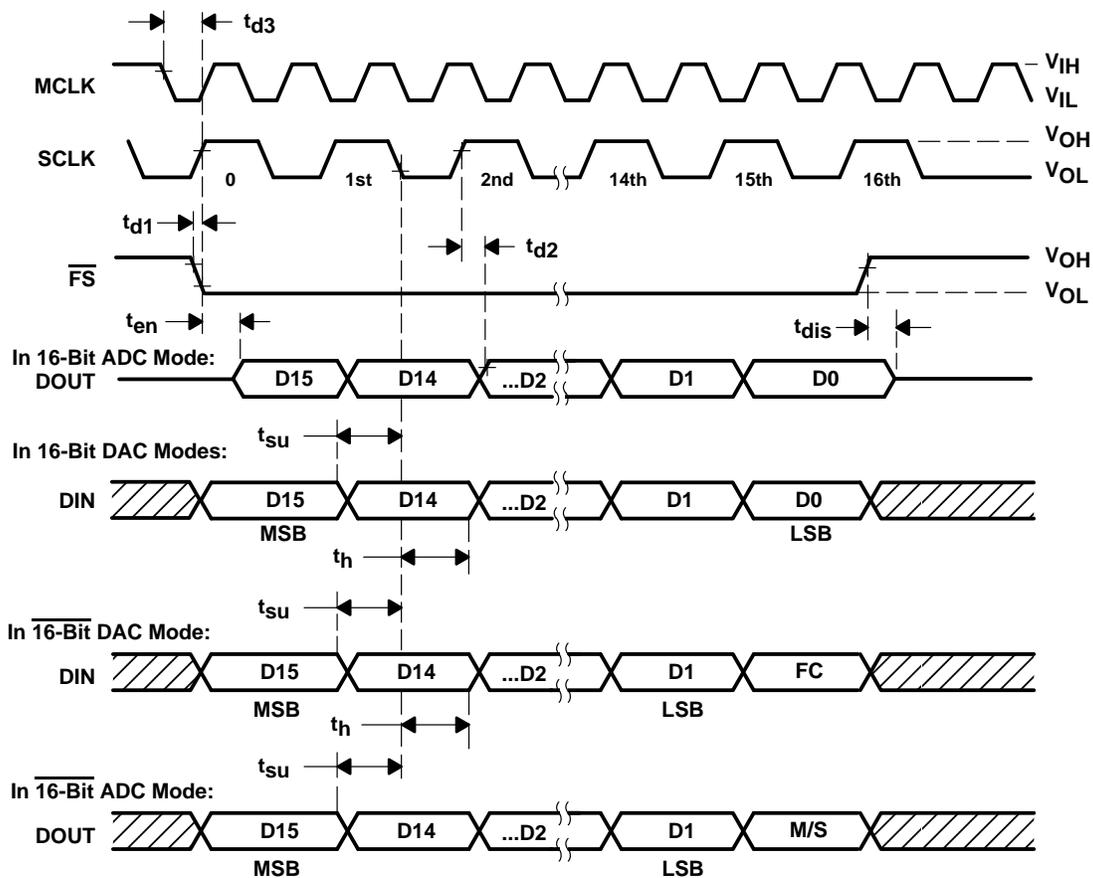


Figure 3–1. Primary Serial Communication Timing

When a secondary request is made through the LSB of the DAC data word (16-bit mode), the format in Table 3–1 is used.

Table 3–1. Secondary Request Format

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|---------|
| ← 15-bit DAC → | | | | | | | | | | | | | | | control |
| ← 2's-complement format → | | | | | | | | | | | | | | | |
| ← 16-bit ADC → | | | | | | | | | | | | | | | |
| ← 2's-complement format → | | | | | | | | | | | | | | | |

3.2 Secondary Serial Communication

Secondary serial communication is used to read or write 16-bit words that program both the options and the circuit configurations of the device. All register programming occurs during secondary communication. Four primary and secondary communication cycles are required to program the four registers. If the default value for a particular register is desired, then the user could omit addressing it during secondary communication. The NOOP command addresses a pseudo-register, register 0, and no register programming takes place during this secondary communication. If a secondary communication is desired for any device, then a secondary communication must be requested for all devices starting with the master. This results in a secondary frame sync for all devices. NOOP commands can be used for devices that do not need a secondary operation.

There are two methods for initiating secondary communications. They are 1) by asserting a high level on FC, or 2) by asserting the LSB of the DIN 16-bit serial communication high while not in 16-bit mode (see Control 1 register, bit 0). Both methods are illustrated in Figure 3-2. Figures 3-3 and 3-4 show the two different ways FC requests secondary communication words as well as the timing for \overline{FS} , DOUT, DIN, and SCLK. The examples span two primary communication frames.

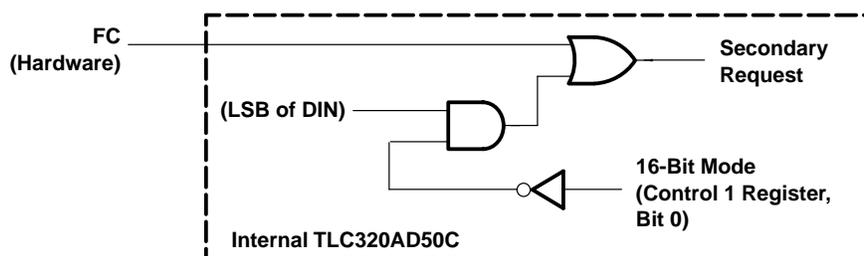


Figure 3-2. Hardware and Software Ways to Make a Secondary Request

The first method for secondary communication asserts FC high. Figure 3-3 shows the use of hardware function control.

During a secondary communication, a register may be written to or read from. When writing a value to a register, the DIN line contains the value to be written. The data returned on DOUT is 00H.

FC should be pulled high before the rising edge of the frame sync (\overline{FS}). This causes the start of the secondary communication 128 SCLKs after the start of the primary communication frame. Read and write examples are shown for DIN and DOUT. If slave devices are present, FC should remain high until the rising edge of the frame sync for the last slave.

The second method for secondary communication asserts the LSB high. Figure 3-4 shows the use of software function control.

A software request is typically used when the required resolution of the DAC channel is less than 16 bits. Then the least significant bit (D0) can be used for the secondary requests as shown in Table 3-2. The request is made by putting the device in 15-bit DAC mode and making the LSB of DIN high. All devices should be in 15-bit DAC mode and secondary communication should be requested for all devices.

Table 3-2. Least Significant Bit Control Function

| CONTROL BIT D0 | CONTROL BIT FUNCTION |
|----------------|---------------------------------|
| 0 | No operation (NOOP) |
| 1 | Secondary communication request |

On the falling edge of the next \overline{FS} , D15-D1 is input to DIN or D15-D0 is output DOUT. If a secondary communication request is made, \overline{FS} goes low after 128 SCLKs after the beginning of the primary frame.

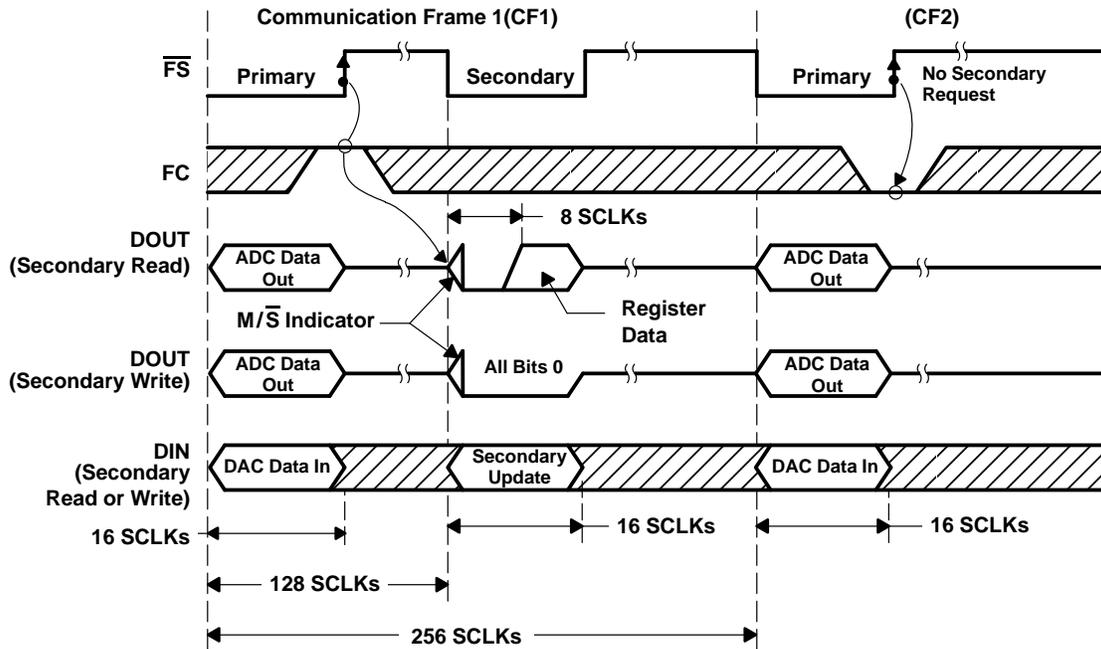
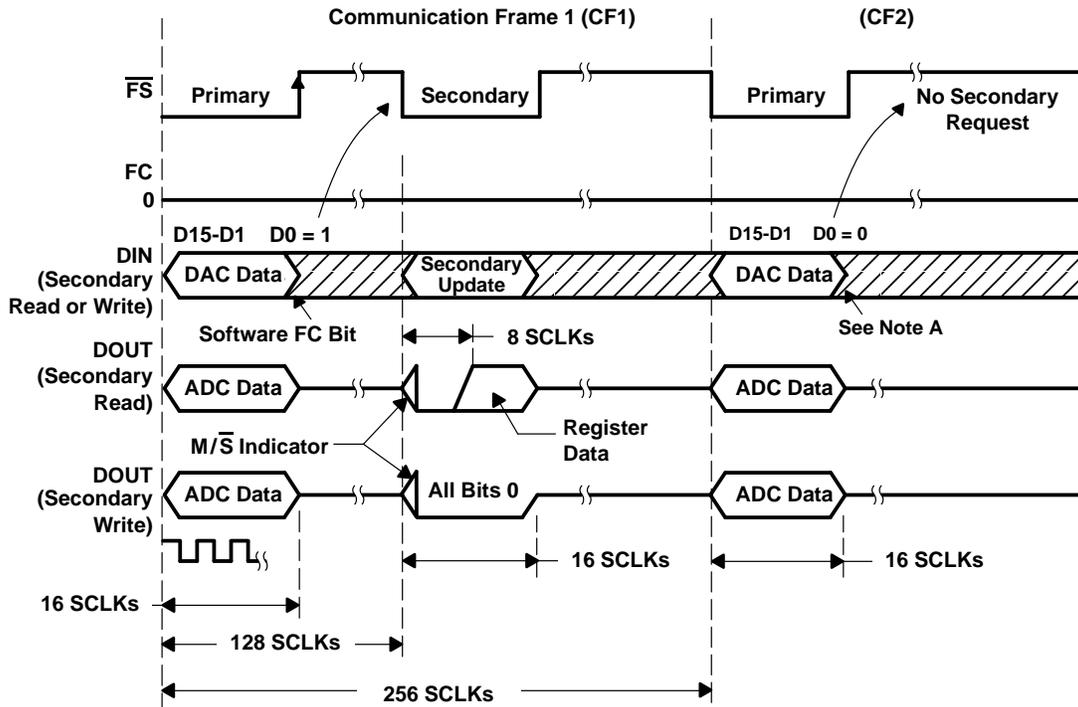


Figure 3–3. Hardware FC Secondary Request

In Figure 3–4, FC hardware terminal 15 is left in its nonasserted state (0). FC is asserted through software by embedding an asserted high level (1) in the LSB of the 16-bit primary word. This is possible when not in 16-bit DAC mode (Control 1 register bit 2 = 0) because the user is using only 15 bits of DAC information.



NOTE A: For a read cycle, the last 8 bits are don't-care bits.

Figure 3–4. Software FC Secondary Request

Table 3–3 shows the secondary communications format. D13 is the read/not write ($\overline{R/W}$) bit.

D12 – D8 are address bits. The register map is specified in the register set section in Appendix A. D7 – D0 are data bits. The data bits are the new values for the specified register addressed by D12–D8.

Table 3–3. Secondary Communication Data Format

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|------------------|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| — | — | $\overline{R/W}$ | A | A | A | A | A | D | D | D | D | D | D | D | D |

3.3 Conversion Rate Versus Serial Port

The SCLK frequency is set equal to the frequency of the frame-sync signal (\overline{FS}) multiplied by 256. The conversion rate or sample rate is equal to the frequency of \overline{FS} .

3.4 Phone Mode Control

Phone mode control is provided for applications that need hardware control and monitoring of external events. By allowing the device to drive the FLAG terminal (set through Control 2 register), the host DSP is capable of system control through the same serial port that connects the device. Along with this control is the capability of monitoring the value of the ALTDATA terminal during a secondary communication cycle. One application for this function is in monitoring RING DETECT or OFFHOOK DETECT from a phone answering system. FLAG allows response to these incoming control signals. Figure 3-5 shows the timing associated with this operating mode.

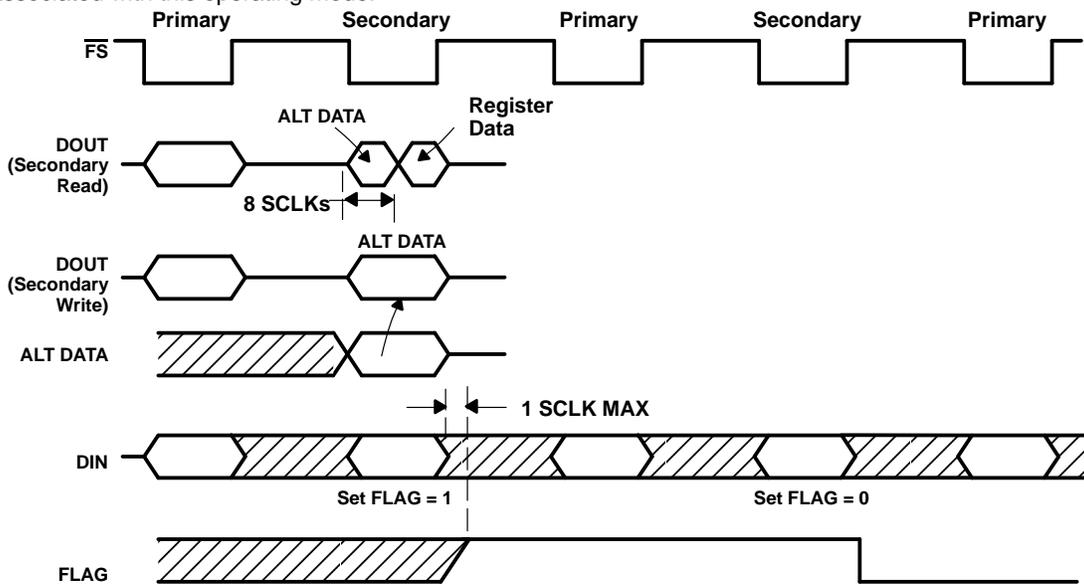


Figure 3-5. Phone Mode Timing

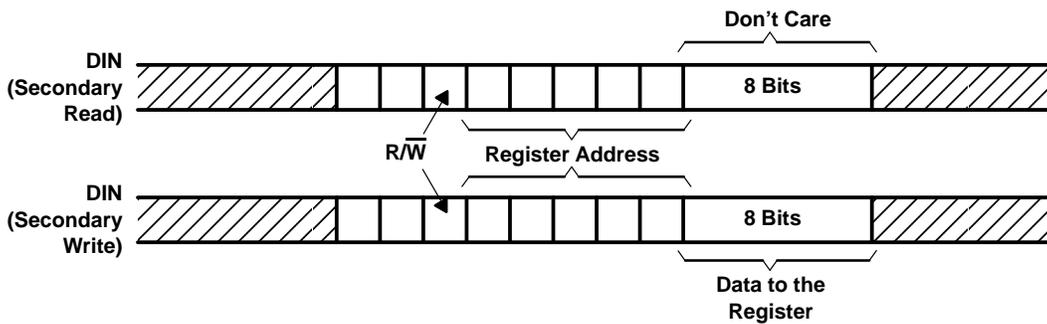


Figure 3-6. Secondary DIN Format

4 Specifications

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

| | |
|---|-----------------------------|
| Supply voltage range, DV_{DD} , AV_{DD} (see Note 1) | -0.3 V to 7 V |
| Output voltage range, DO_{UT} , \overline{FS} , $SCLK$, $FLAG0$, $FLAG1$ | -0.3 V to $DV_{DD} + 0.3$ V |
| Output voltage range, $OUTP$, $OUTM$ | -0.3 V to $V_{DD} + 0.3$ V |
| Input voltage range, DIN , \overline{PWRDWN} , \overline{RESET} , $ALTDATA$, MCLK, FC | -0.3 V to $DV_{DD} + 0.3$ V |
| Input voltage range, INP , INM , $AUXP$, $AUXM$ | -0.3 V to $V_{DD} + 0.3$ V |
| Case temperature for 10 seconds: DW package | 260°C |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

4.2 Recommended Operating Conditions

| | MIN | NOM | MAX | UNIT |
|---|------|-----|-------|----------|
| Supply voltage, AV_{DD} (see Note 2) | 4.75 | | 5.5 | V |
| Analog signal voltage (V_I) | | | 6 | V |
| Differential, (INP–INM) peak, for full scale operation | | | | |
| Differential output load resistance, $OUTP$, $OUTM$, R_L | 600 | | | Ω |
| Differential output load capacitance, $OUTP$, $OUTM$, C_L | | | 15 | pF |
| ADC or DAC conversion rate | | 8 | 22.05 | kHz |
| Operating free-air temperature, T_A | 0 | | 70 | °C |

NOTE 2: Voltages at analog inputs and outputs and V_{DD} are with respect to the V_{SS} terminal.

4.2.1 Recommended Operating Conditions, $DV_{DD} = 5$ V

| | MIN | NOM | MAX | UNIT |
|--|-----|-------|--------|------|
| Supply voltage, DV_{DD} (see Note 2) | 4.5 | | 5.5 | V |
| High-level input voltage, V_{IH} | 2 | | | V |
| Low-level input voltage, V_{IL} | | | 0.8 | V |
| MCLK frequency | | 8.192 | 22.579 | MHz |

NOTE 2: Voltages at analog inputs and outputs and V_{DD} are with respect to the V_{SS} terminal.

4.2.2 Recommended Operating Conditions, $DV_{DD} = 3$ V

| | MIN | NOM | MAX | UNIT |
|--|-----|-------|--------|------|
| Supply voltage, DV_{DD} (see Note 2) | 2.7 | 3 | 3.3 | V |
| High-level input voltage, V_{IH} | 1.8 | | | V |
| Low-level input voltage, V_{IL} | | | 0.6 | V |
| MCLK frequency | | 8.192 | 22.579 | MHz |

NOTE 2: Voltages at analog inputs and outputs and V_{DD} are with respect to the V_{SS} terminal.

4.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted)

4.3.1 Digital Inputs and Outputs, $MCLK = 8.192\text{ MHz}$, $f_s = 8\text{ kHz}$, Outputs Not Loaded

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------|-----|-----|-----|---------------|
| V_{OH} High-level output voltage, DOUT | $I_O = 360\ \mu\text{A}$ | 2.4 | 4.6 | | V |
| V_{OL} Low-level output voltage, DOUT | $I_O = 2\text{ mA}$ | | 0.2 | 0.4 | V |
| I_{IH} High-level input current, any digital input | $V_{IH} = 5\text{ V}$ | | | 10 | μA |
| I_{IL} Low-level input current, any digital input | $V_{IL} = 0.8\text{ V}$ | | | 10 | μA |
| C_i Input capacitance | | | 5 | | pF |
| C_o Output capacitance | | | 5 | | pF |

4.3.2 Digital Inputs and Outputs, $MCLK = 8.192\text{ MHz}$, $f_s = 8\text{ kHz}$, Outputs Not Loaded, $V_{DD} = 3\text{ V}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------|-----|-----|-----|---------------|
| V_{OH} High-level output voltage, DOUT | $I_O = 360\ \mu\text{A}$ | 2 | | | V |
| V_{OL} Low-level output voltage, DOUT | $I_O = 2\text{ mA}$ | | | 0.4 | V |
| I_{IH} High-level input current, any digital input | $V_{IH} = 3.3\text{ V}$ | | | 10 | μA |
| I_{IL} Low-level input current, any digital input | $V_{IL} = 0.6\text{ V}$ | | | 10 | μA |
| C_i Input capacitance | | | 5 | | pF |
| C_o Output capacitance | | | 5 | | pF |

4.3.3 ADC Path Filter, $MCLK = 8.192\text{ MHz}$, $f_s = 8\text{ kHz}$ (see Note 3)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------------|-------|-----|------|------|
| Filter gain relative to gain at 1020 Hz | 0 to 300 Hz | -0.5 | | 0.2 | dB |
| | 300 Hz to 3 kHz | -0.25 | | 0.25 | |
| | 3.3 kHz | -0.35 | | 0.3 | |
| | 3.6 kHz | | | -3 | |
| | 4 kHz | | | -40 | |
| | $\geq 4.4\text{ kHz}$ | | | -74 | |

NOTE 3: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dB = 6 V_{PP} differential as the reference level for the analog input signal. The passband is 0 to 3400 Hz for an 8-kHz sample rate. The passband scales linearly with the sample rate.

4.3.4 ADC Dynamic Performance, $MCLK = 8.192\text{ MHz}$, $f_s = 8\text{ kHz}$

4.3.4.1 ADC Signal-to-Noise (see Note 4)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|-------------------------------|-----|-----|-----|------|
| Signal-to-noise ratio (SNR) | $V_I = -1\text{ dB}$ (5.35 V) | 85 | 89 | | dB |
| | $V_I = -9\text{ dB}$ (2.13 V) | 77 | 81 | | |
| | $V_I = -40\text{ dB}$ (60 mV) | 46 | 50 | | |
| | $V_I = -65\text{ dB}$ (3 mV) | 21 | 25 | | |
| | $V_{AUX} = -9\text{ dB}$ | 77 | 81 | | |

NOTE 4: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $AV_{DD}/2$.

4.3.4.2 ADC Signal-to-Distortion (see Note 4)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------------------|-----|-----|-----|------|
| Signal-to-total harmonic distortion (THD) | $V_I = -3$ dB (4.25 V) | 80 | 85 | | dB |
| | $V_I = -9$ dB (2.13 V) | 79 | 90 | | |
| | $V_I = -40$ dB (60 mV) | 67 | 72 | | |
| | $V_I = -65$ dB (3 mV) | 43 | 48 | | |
| | $V_{AUX} = -9$ dB | 79 | 90 | | |

NOTE 4. The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.3.4.3 ADC Signal-to-Distortion + Noise (see Note 4)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------------------|-----|-----|-----|------|
| Total harmonic distortion + noise (THD + N) | $V_I = -3$ dB (4.25 V) | 78 | 82 | | dB |
| | $V_I = -9$ dB (2.13 V) | 76 | 80 | | |
| | $V_I = -40$ dB (60 mV) | 45 | 49 | | |
| | $V_I = -65$ dB (3 mV) | 20 | 24 | | |
| | $V_{AUX} = -9$ dB | 76 | 80 | | |

NOTE 4. The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.3.5 ADC Channel

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---------------------------|-----|-----------|-----|-------------|
| $V_{I(PP)}$ Peak-to-peak input voltage | | | 6 | | V |
| Dynamic range | $V_I = -1$ dB (5.35 V) | | 88 | | dB |
| Interchannel isolation | | | 100 | | |
| E_G Gain error | $V_I = -1$ dB at 1020 Hz | | ± 0.3 | | |
| $E_{O(ADC)}$ ADC converter off set error | | | 5 | | mV |
| CMRR Common-mode rejection ratio at INM, INP or AUXM, AUXP | $V_I = -1$ dB at 1020 kHz | | 74 | | dB |
| Idle channel noise (on-chip reference) | $V_{INP}, INM = 2.5$ V | | | 75 | μ V rms |
| R_i Input resistance | $T_A = 25^\circ\text{C}$ | 70 | 100 | | k Ω |
| Channel delay | | | $17/f_S$ | | s |

4.3.6 DAC Path Filter, MCLK = 8.192 MHz, $f_S = 8$ kHz (see Note 5)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-------|-----|------|------|
| Filter gain relative to gain at 1020 Hz | 0 to 300 Hz | -0.5 | | 0.2 | dB |
| | 300 Hz to 3 kHz | -0.25 | | 0.25 | |
| | 3.3 kHz | -0.35 | | 0.3 | |
| | 3.6 kHz | | | -3 | |
| | 4 kHz | | | -40 | |
| | ≥ 4.4 kHz | | | -74 | |

NOTE 5: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V_{PP} . The passband is 0 to 3600 Hz.

4.3.7 DAC Dynamic Performance

4.3.7.1 DAC Signal-to-Noise (see Note 6)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------|-----|-----|-----|------|
| Signal-to-noise ratio (SNR) | $V_O = 0$ dB | 85 | 89 | | dB |
| | $V_O = -9$ dB | 76 | 80 | | |
| | $V_O = -40$ dB | 45 | 49 | | |
| | $V_O = -65$ dB | 20 | 24 | | |

NOTE 6: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.7.2 DAC Signal-to-Distortion (see Note 6)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-----|-----|------|
| Signal-to-total harmonic distortion (THD) | $V_O = -3$ dB | 76 | 80 | | dB |
| | $V_O = -9$ dB | 84 | 90 | | |
| | $V_O = -40$ dB | 64 | 72 | | |
| | $V_O = -65$ dB | 42 | 48 | | |

NOTE 6: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.7.3 DAC Signal-to-Noise+Distortion (see Note 6)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-----|-----|------|
| Total harmonic distortion + noise (THD + N) | $V_O = -3$ dB | 75 | 79 | | dB |
| | $V_O = -9$ dB | 75 | 79 | | |
| | $V_O = -40$ dB | 45 | 49 | | |
| | $V_O = -65$ dB | 20 | 24 | | |

NOTE 6: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of application schematic low-pass filter. The test is conducted in 16-bit mode.

4.3.8 DAC Channel

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-----------|-----|-----------------|
| Dynamic range | | | 88 | | dB |
| Interchannel isolation | | | 100 | | |
| E_G Gain error, 0 dB | $V_O = 0$ dB at 1020 Hz | | ± 0.3 | | |
| Idle channel broadband noise | See Note 7 | | | 175 | μV rms |
| Idle channel narrow band noise | 0 – 4 kHz, See Note 7 | | | 125 | μV rms |
| V_{OO} Output offset voltage at OUT (differential) | DIN = All 0s | | 30 | | mV |
| V_O Analog output voltage, OUTP–OUTM | $R_L = 600 \Omega$ max (see Figure 3–8) with internal reference and full-scale digital input, see Note 8, differential | | | 6 | V _{PP} |
| Total out of band energy (0.55 f_S to 3 MHz) | | | | -45 | dB |
| Channel delay | | | $18/f_S$ | | s |

NOTES: 7. The conversion rate is 8 kHz; the-out-of-band measurement is made from 4400 Hz to 3 MHz.

8. The digital input to the DAC channel at DIN is in 2's complement. The TLC320AD50C is a current DAC and requires a load resistor for current to voltage conversion.

4.3.9 Power Supplies, $AV_{DD} = DV_{DD} = 5\text{ V}$, No Load

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--|-----------------|-----|-----|-----|------|
| I_{DD} (analog) | Power supply current, ADC | Operating | | 18 | 24 | mA |
| | | Power down | | 1 | | |
| I_{DD} (PLL) | Power supply current, PLL | Operating | | 2 | 4 | mA |
| | | Power down | | 0.5 | | |
| I_{DD} (digital 1) | Power supply current, digital | Operating | | 4 | 7 | mA |
| | | Power down | | 10 | | |
| I_{DD} (digital 2) | Power supply current, digital, $DV_{DD} = 3.3\text{ V}$ | Operating | | 4 | | mA |
| | | Power down | | 10 | | |
| P_D | Power dissipation | Operating | | 120 | 175 | mW |
| | | H/W-power down | | 7.5 | 20 | |

4.3.10 Power-Supply Rejection, $AV_{DD} = DV_{DD} = 5\text{ V}$ (see Note 9)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-----------|---|----------------------|-----|------|-----|------|
| AV_{DD} | Supply voltage rejection ratio, analog supply | $f_i = 0$ to $f_s/2$ | | 50 | | dB |
| DV_{DD} | Supply voltage rejection ratio, DAC channel | $f_i = 0$ to 30 kHz | | 40 | | |
| | Supply voltage rejection ratio, ADC channel | $f_i = 0$ to 30 kHz | | 50 | | |

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 9: Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

4.4 Timing Requirements

4.4.1 Master Mode Timing Requirements

| | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--|----------------------|-----|-----|-----|------|
| t_{d1} | Delay time, $SCLK\uparrow$ to $\overline{FS}\downarrow$ | $C_L = 20\text{ pF}$ | | | 0 | ns |
| t_{d2} | Delay time, $SCLK\uparrow$ to DOUT | | | | 20 | |
| t_{su1} | Setup time, DIN, before $SCLK$ low | | 25 | | | |
| t_{h1} | Hold time, DIN, after $SCLK$ high | | | | 20 | |
| t_{en1} | Enable time, $\overline{FS}\downarrow$ to DOUT | | | | 25 | |
| t_{dis1} | Disable time, $\overline{FS}\uparrow$ to DOUT hi-Z | | | 20 | | |
| t_{d3} | Delay time, $MCLK\downarrow$ to $SCLK\uparrow$ | | | | 50 | |
| $t_{d(CH-FL)}$ | Delay time, $SCLK$ high to \overline{FSD} low (see Figure 5-1) | | | | 50 | |
| t_{wH} | Pulse duration, MCLK high | | | 32 | | |
| t_{wL} | Pulse duration, MCLK low | | | 20 | | |

4.4.2 Slave Mode Timing Requirements

| | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|-----|-----|-----|------|
| t _{d4} | Delay time, SCLK↑ to \overline{FS} ↓ | | | 0 | ns |
| t _{d5} | Delay time, SCLK↑ to DOUT | | | 20 | |
| t _{su2} | Setup time, DIN, before SCLK low | 20 | | | |
| t _{h2} | Hold time, DIN, after SCLK high | | | 20 | |
| t _{en2} | Enable time, \overline{FS} ↓ to DOUT | | | 25 | |
| t _{dis2} | Disable time, \overline{FS} ↑ to DOUT hi-Z | | 20 | | |
| t _{d6} | Delay time, MCLK↓ to SCLK↑ | | | 50 | |
| t _d (FL-FDL) | Delay time, \overline{FS} low to \overline{FSD} low, slave to slave (see Figure 5-2) | | | 40 | |
| t _d (CH-FDL) | Delay time, SCLK high to \overline{FSD} low, slave mode (see Figure 5-3) | | | 50 | |
| t _{wH} | Pulse duration, MCLK high | 32 | | | |
| t _{wL} | Pulse duration, MCLK low | 20 | | | |

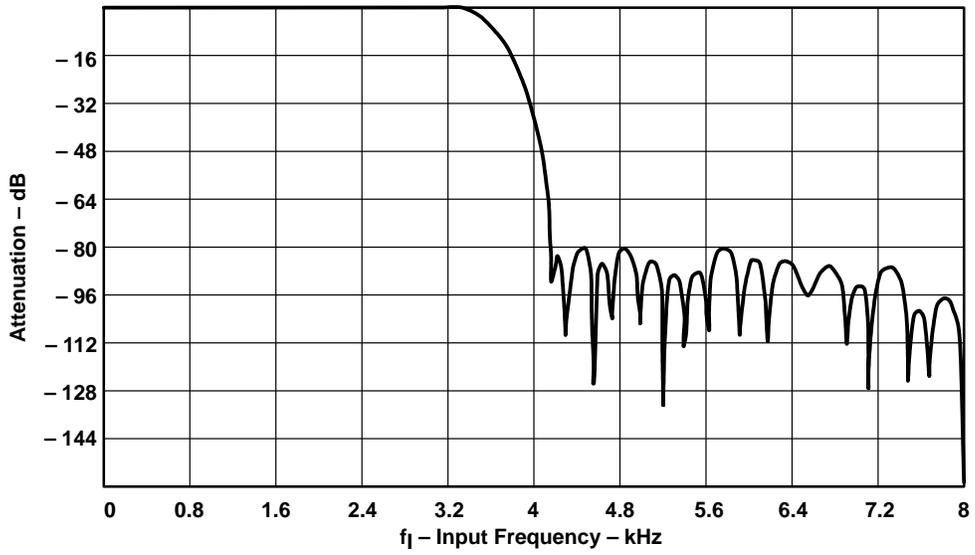


Figure 4 –1. ADC Decimation Filter Response

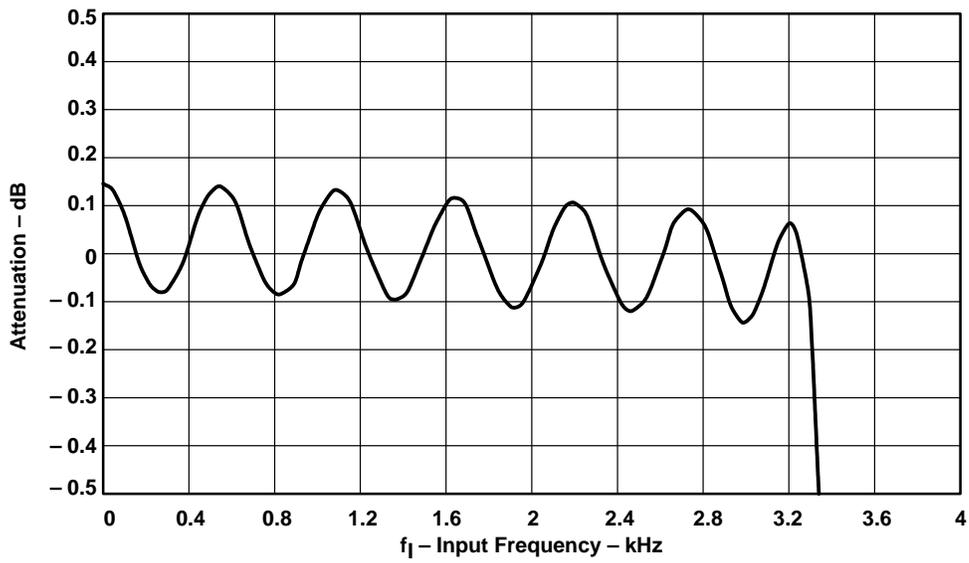


Figure 4 –2. ADC Decimation Filter Passband Ripple

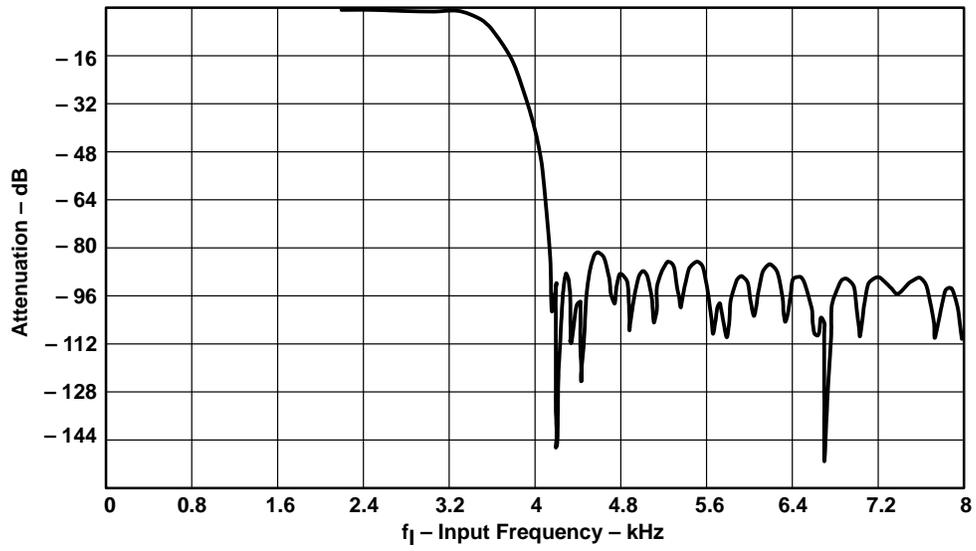


Figure 4-1. DAC Interpolation Filter Response

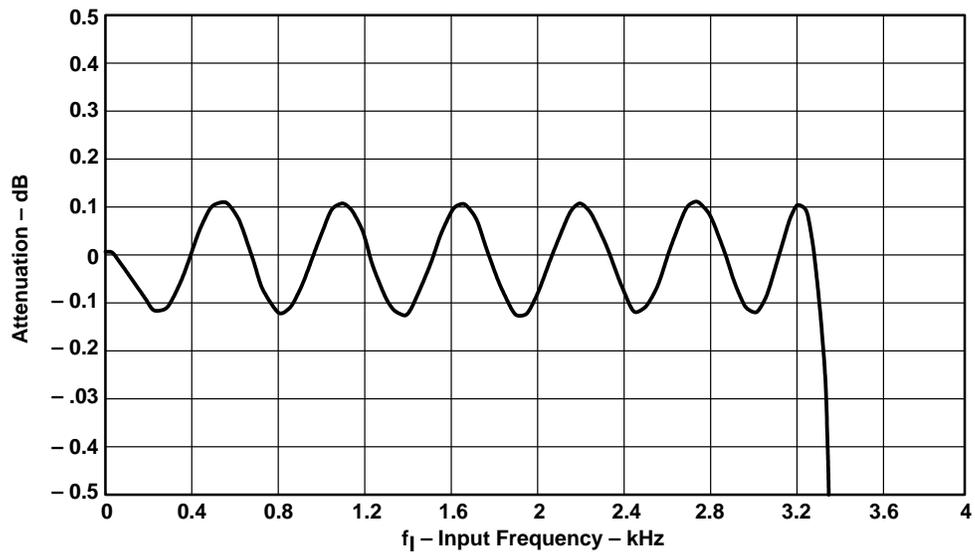


Figure 4-2. DAC Interpolation Filter Passband Ripple

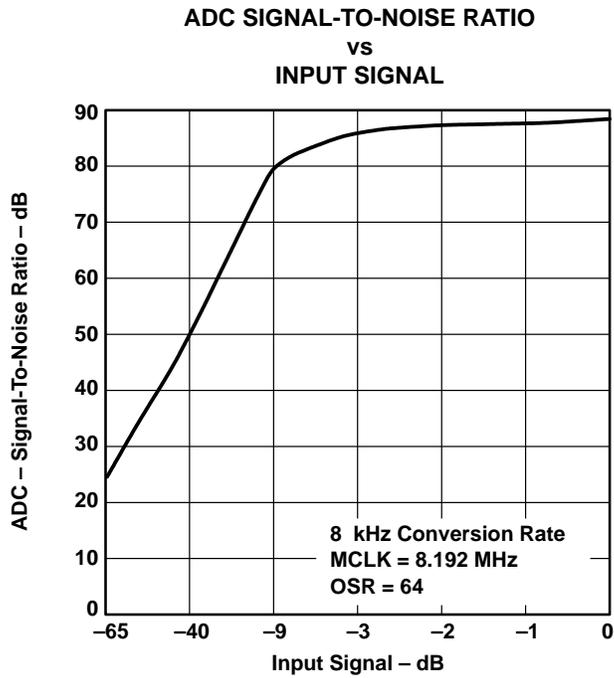


Figure 4-3.

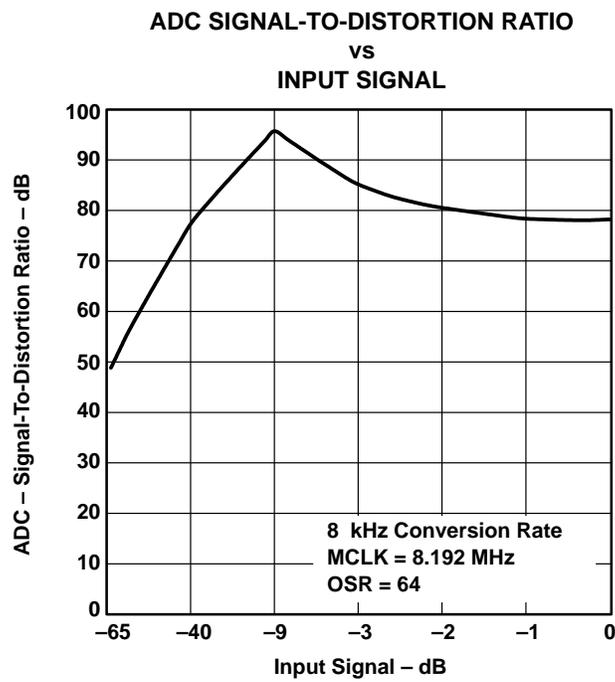


Figure 4-4.

ADC SIGNAL-TO-(NOISE AND DISTORTION) RATIO
vs
INPUT SIGNAL

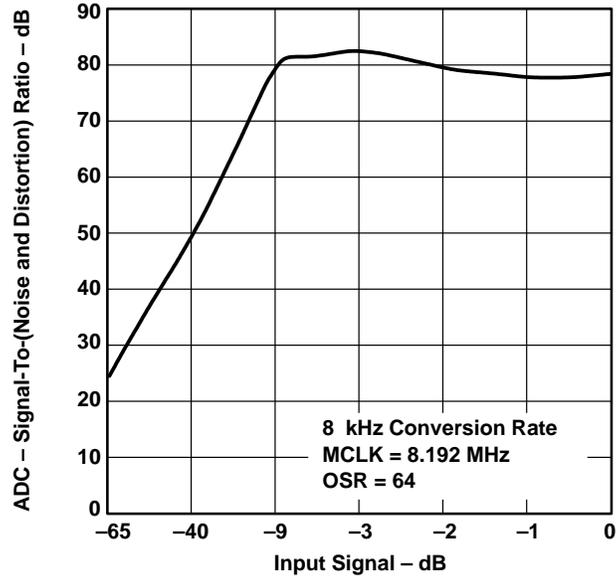


Figure 4-5.

DAC SIGNAL-TO-NOISE RATIO
vs
INPUT SIGNAL

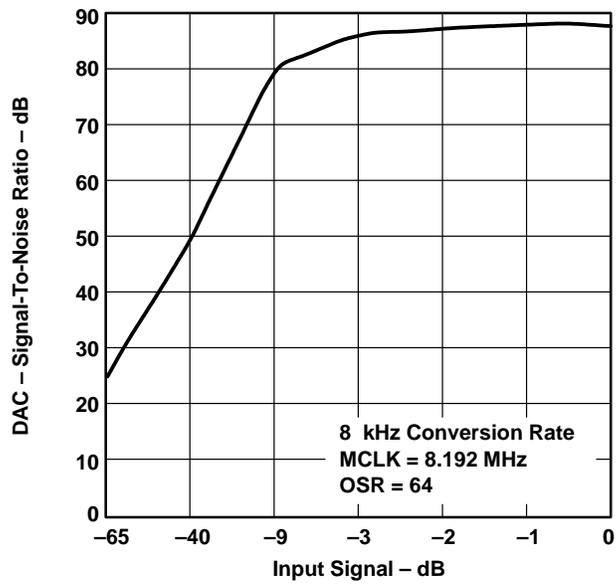


Figure 4-6.

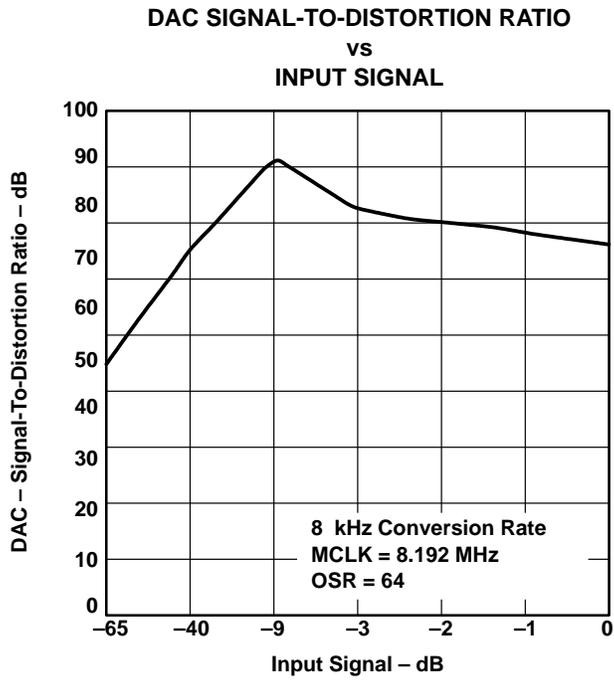


Figure 4-7.

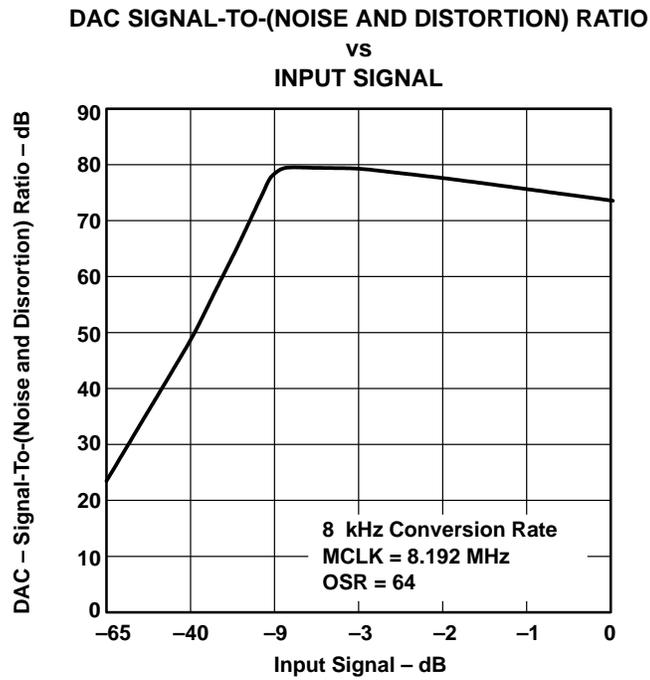
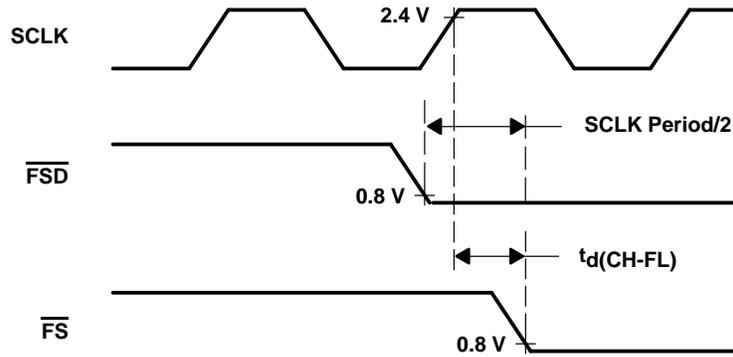


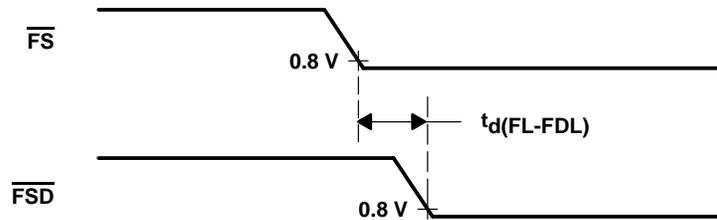
Figure 4-8.

5 Parameter Measurement Information



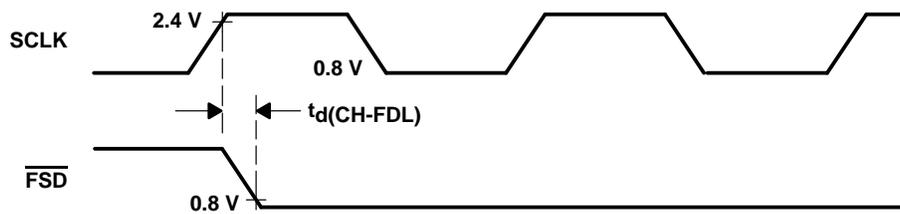
NOTE A: Timing shown is for the TLC320AD50C operating as the master or as a stand-alone device.

Figure 5–1. Master or Stand-Alone \overline{FS} and \overline{FSD} Timing



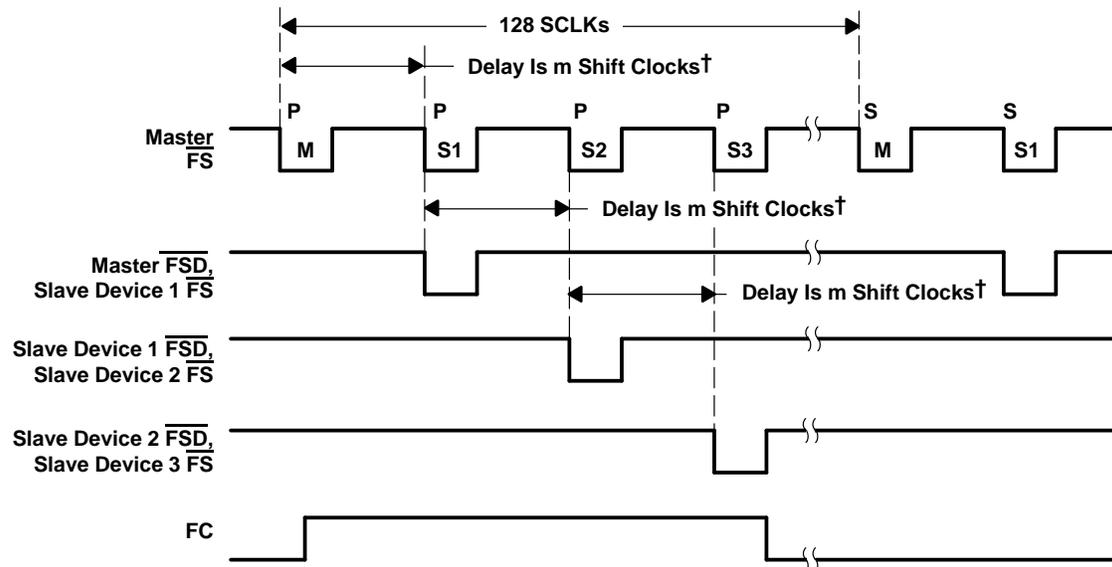
NOTE A: Timing shown is for the TLC320AD50C operating in the slave mode (\overline{FS} and SCLK signals are generated externally). The programmed data value in the FSD register is 0.

Figure 5–2. Slave \overline{FS} to \overline{FSD} Timing



NOTE A: Timing shown is for the TLC320AD50C operating in the slave mode (\overline{FS} and SCLK signals are generated externally). There is a data value in the FSD register greater than 18 decimal.

Figure 5–3. Slave SCLK to \overline{FSD} Timing



† The delay time from any \overline{FS} signals to the corresponding \overline{FSD} signals is m shift clocks with the value of m being the numerical value of the data programmed into the FSD register. In the master mode with slaves, the same data word programs the master and all slave devices; therefore, master to slave 1, slave 1 to slave 2, slave 2 to slave 3, etc., have the same delay time.

Figure 5–4. Master-Slave Frame-Sync Timing After a Delay Has Been Programmed Into the FSD Registers

6 Application Information

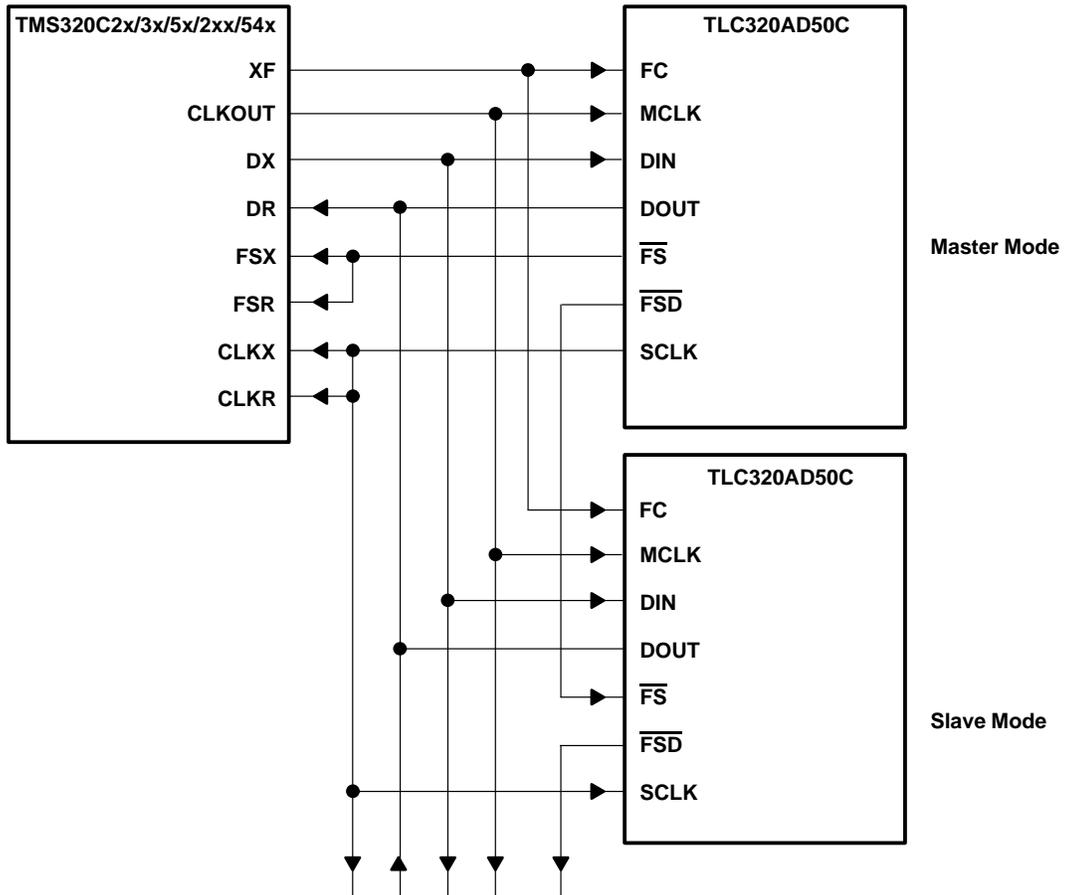


Figure 6–1. Master Device and Slave Device Connections (to DSP Interface)

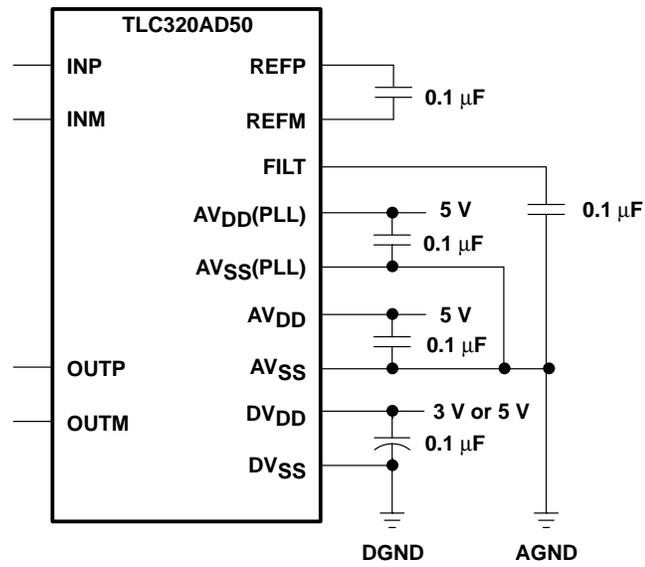


Figure 6–2. Power Supply Decoupling

Appendix A Register Set

Bits D12 through D8 in a secondary serial communication comprise the address of the register that is written with data carried in D7 through D0. D13 determines a read or write cycle to the addressed register. When low, a write cycle is selected.

The following table shows the register map.

Table A–1. Register Map

| REGISTER NO. | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | REGISTER NAME |
|--------------|-----|-----|-----|-----|-----|-----|----|----|---------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No operation |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Control 1 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Control 2 |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Control 3 |
| 4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Control 4 |

Control 1 Register

Table A–2. Control 1 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|---|
| 1 | – | – | – | – | – | – | – | Software reset |
| 0 | – | – | – | – | – | – | – | Software reset not asserted |
| – | 1 | – | – | – | – | – | – | Software power down (analog and filters) |
| – | 0 | – | – | – | – | – | – | Software power down (not asserted) |
| – | – | 1 | – | – | – | – | – | Select AUXP and AUXM for ADC |
| – | – | 0 | – | – | – | – | – | Select INP and INM for ADC |
| – | – | – | 0 | – | – | – | – | Select INP and INM for monitor |
| – | – | – | 1 | – | – | – | – | Select AUXP and AUXM for monitor |
| – | – | – | – | 1 | 1 | – | – | Monitor amplifier gain = –18 dB (see Note 1) |
| – | – | – | – | 1 | 0 | – | – | Monitor amplifier gain = –8 dB (see Note 1) |
| – | – | – | – | 0 | 1 | – | – | Monitor amplifier gain = 0 dB (see Note 1) |
| – | – | – | – | 0 | 0 | – | – | Monitor amp mute |
| – | – | – | – | – | – | 1 | – | Digital loopback asserted |
| – | – | – | – | – | – | 0 | – | Digital loopback not asserted |
| – | – | – | – | – | – | – | 1 | 16-bit DAC mode (hardware secondary requests) |
| – | – | – | – | – | – | – | 0 | Not 16-bit DAC mode (software secondary requests) |

Default value: 0 0 0 0 0 0 0 0

NOTE 1: These gains are for a single-ended input. The gain is 6 dB lower with a differential input.

A software reset is a one-shot operation and this bit is cleared to 0 after reset. It is not necessary to write a 0 to end the master reset operation. Writing 0s to the reserved bits is suggested.

Control 2 Register

Table A-3. Control 2 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--|
| X | – | – | – | – | – | – | – | FLAG output value |
| – | 1 | – | – | – | – | – | – | Phone mode enable |
| – | 0 | – | – | – | – | – | – | Phone mode disable |
| – | – | X | – | – | – | – | – | Decimator FIR overflow flag (valid only during read cycle) |
| – | – | – | 1 | – | – | – | – | 16-bit ADC mode |
| – | – | – | 0 | – | – | – | – | Not-16-bit ADC mode |
| – | – | – | – | – | X | X | X | Reserved |
| – | – | – | – | 1 | – | – | – | Analog loopback enabled |
| – | – | – | – | 0 | – | – | – | Analog loopback disabled |

Default value: 00000000

Writing 0s to the reserved bits is suggested.

Control 3 Register

The following command contains the frame-sync delay (FSD) register address and loads $\overline{D7}$ (MSB)– $\overline{D0}$ into the FSD register. The data byte ($\overline{D1}$ – $\overline{D0}$) determines the number of SCLKs between \overline{FS} and the delayed frame-sync signal, \overline{FSD} . The minimum data value for the register is decimal 18.

Table A-4. Control 3 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|--|
| – | – | X | X | X | X | X | X | Number of SCLKs between \overline{FS} and \overline{FSD} |
| X | X | – | – | – | – | – | – | Binary number of slave devices (3 max) |

Default value: 00000000

Writing 0s to the reserved bits is suggested.

Control 4 Register

Table A-5. Control 4 Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DESCRIPTION |
|----|----|----|----|----|----|----|----|---|
| - | - | - | - | 1 | 1 | - | - | Analog input gain = mute |
| - | - | - | - | 1 | 0 | - | - | Analog input gain = 12 dB |
| - | - | - | - | 0 | 1 | - | - | Analog input gain = 6 dB |
| - | - | - | - | 0 | 0 | - | - | Analog input gain = 0 dB |
| - | - | - | - | - | - | 1 | 1 | Analog output gain = mute |
| - | - | - | - | - | - | 1 | 0 | Analog output gain = - 12 dB |
| - | - | - | - | - | - | 0 | 1 | Analog output gain = - 6 dB |
| - | - | - | - | - | - | 0 | 0 | Analog output gain = 0 dB |
| - | X | X | X | - | - | - | - | Sample frequency select (N): $f_s = \text{MCLK}/(128 \times N)$ or $\text{MCLK}/(512 \times N)$ |
| 1 | - | - | - | - | - | - | - | External sample clock feature enabled |
| 0 | - | - | - | - | - | - | - | External sample clock feature disabled |

Default value: 00000000

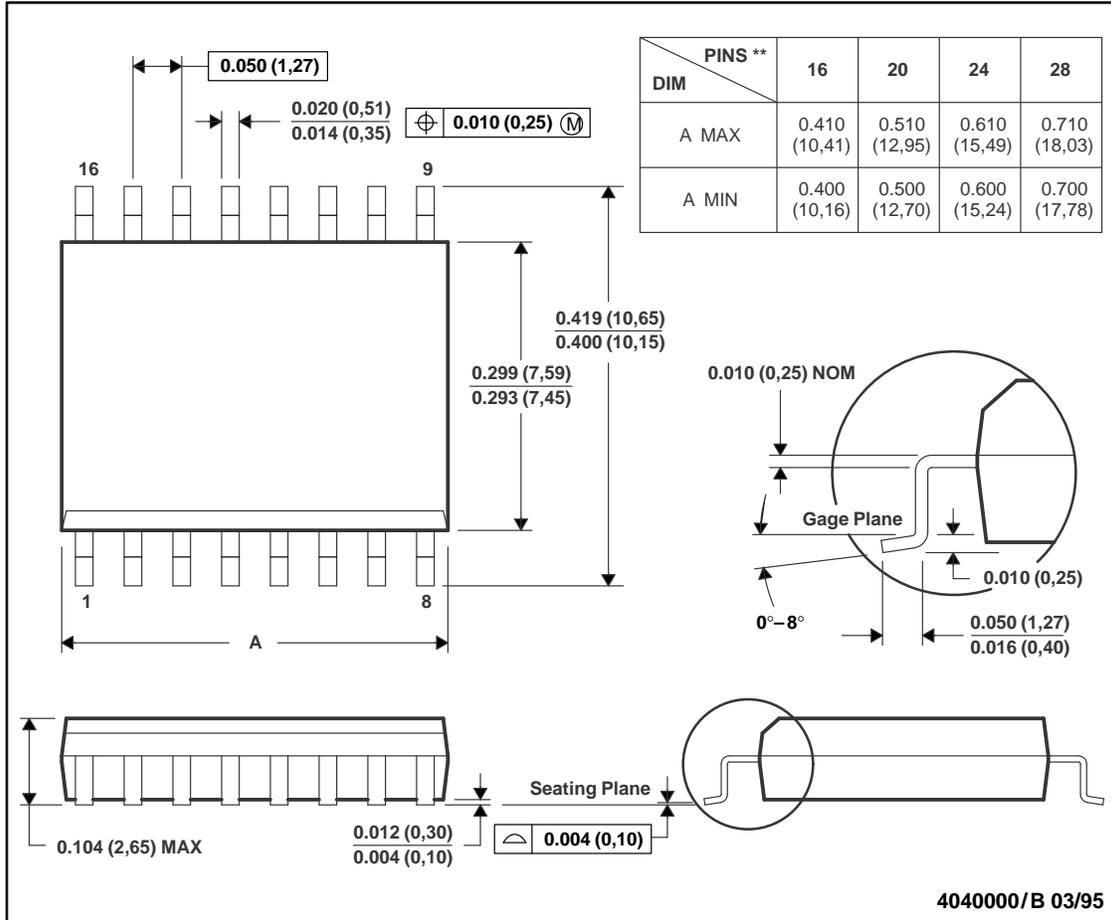
The value of the sample frequency divisor, N, is determined by the octal representation of bits D4 – D6. Hence, 001 = 1, 010 = 2, etc. By setting D4 – D6 to 000, N = 8 is selected.

Appendix B Mechanical Data

DW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

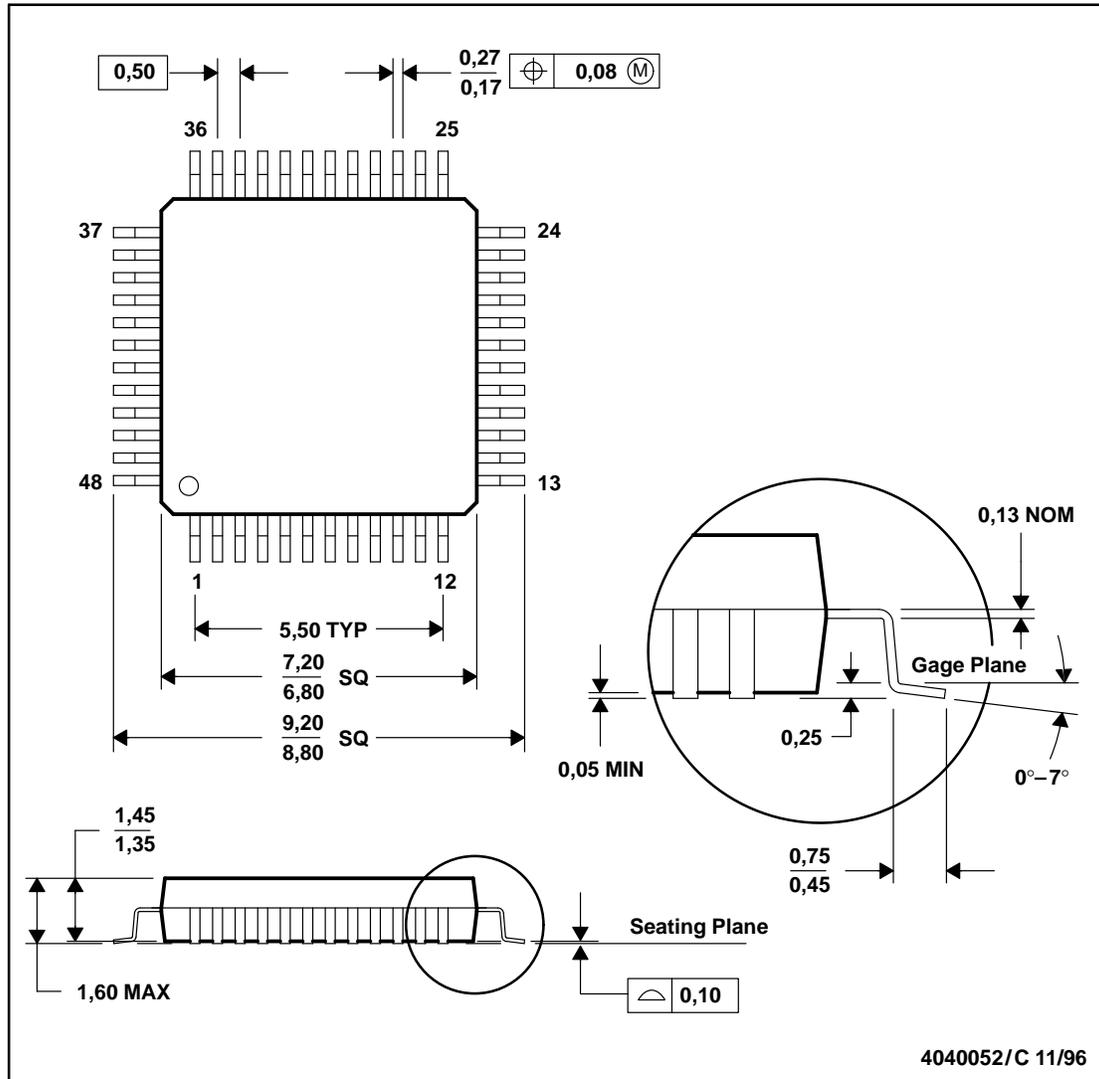
16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

PT (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MO-136
 D. Also may be a thermally enhanced plastic package with leads connected to the die pads

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