Intel® StrongARM® SA-1110 Microprocessor

Specification Update

January 2000

Notice: The SA-1110 may contain design defects or errors known as errata. Characterized errata that may cause the SA-1110's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278259-015

Contents

Revision History

Date	Version	Description
1/25/00	015	Under Documentation Changes, removed documentation changes #63 — #99 (referencing the 014 specification update) from the specification update and applied them to the developer's manual; added two changes documenting a change in the exit idle mode process (Chapter 9) and a change in the register summary table (Appendix A). Under Specification Changes, added one line to Specification Changes table.
1/11/99	014	Under Documentation Changes, added 38 documentation changes removing all references to SDLC, substituting SDLC information with GPCLK information. Made four changes substituting RDN+1 with RDF+1. Changed one line in the parameters definition list in section 10.5.8 and added one footnote for Figure 10-18. Also added GPCLKR0 register to Section 11.9.3.6. Under Errata, added one errata documenting UDC work-around procedure.
12/07/99	013	Under Errata, added nine errata; under Documentation Changes, changed output signals listed in Table 13-2; changes made to Section 10.1.7, Section 10.2.1, Section 10.2.2, Section 10.2.3, Section 10.2.4, Section 10.2.5, Section 10.3, Section 10.4.6, Section 10.5.1, Section 10.5.11, Section 10.7, Section 10.7.1, and Section 10.7.2; changed Section 13.6.SDLC feature changed from an errata to a specification change.
11/18/99	012	Under Documentation Changes, changed ID code and added stepping information in section 5.2.1.
11/15/99	011	Under Errata, added two errata; under Documentation Changes, changed title of section 13.2.
11/05/99	010	Under Documentation Changes, added sentence to end of first paragraph in section 9.5.2.2.
11/03/99	009	Under Documentation Changes, changed signal description of GPIO pin 25 in table in section 9.1.2; added note to end of section 11.11.6; deleted note to bit 3 of the RCSR register in section 9.6.1.2; revised bit 0 description of USB Device Controller (UDC) CR register in section 11.8.3.8; replaced section 11.10.2.3; corrected typo in table 9-3 title; changed sentence in section 10.8.
10/08/99	008	Under Errata, added one errata; under Documentation Changes, added paragraph to section 16.6.3; added boundary-scan signals and pins table 16-2.
09/15/99	007	Under Documentation Changes, added footnote to GPIO Alternate Functions Table in Section 9.1.2.
08/19/99	006	Under Documentation Changes, changed settings for serial port 2 and serial port 4 in Table 11-6.
07/22/99	005	Under Documentation Changes, changed code example for section 6.2.3; changed last sentence of section 9.5.3; added output signals to table 13-2.
06/28/99	004	Under Documentation Changes, removed section 16.8; changed Test Unit Control Register's description of bit 10; added change to Section 9.5.7.7; changed Figure 10-6; added change to section 10.5.1; added change to section 10.1; added change to section 10.2.2.and description of MDREFR:EAPD and MDREFR:KAPD bits; added step #8 to section 10.7.1; removed the SA-1110 Tool Chains and Operating Systems Table from the brief datasheet and the developer's manual; added change to section 9.5.6; added change to section 11.13.1; added change to section 11.13.6; added change to section 10.5.5.

Date	Version	Description
05/18/99	003	Under Documentation Changes, added changes to the PPSR and PSDR register drawing graphics; added changes to the OS Timer Interrupt Enable register; added change to the Big and Little Endian DMA Transfers graphic; corrected peripheral pin assignments; changed 15 timing diagrams; changed bit 31 description in the DRAM Refresh Control Register; added changes to section 10.4.7; added changes to section 10.7.1; added changes to section 10.8.
04/19/99	002	Under Document Changes, added changes to section 1.1; section 9.1.2.1; section 3.1; section 10.2.4; and section 10.6.
03/26/99	001	This is the new specification update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® StrongARM® SA-1110 Microprocessor Developer's Manual	278240-002
Intel® StrongARM® SA-1110 Microprocessor Brief Datasheet	278241-001

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the SA-1110 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	A0	B0	B1			
1	X	X	X	16	No Fix	Incorrect Sign-Extended Value in Register After a Read Buffer Allocate
2	X	X	X	16	No Fix	LCD Ghost Lines
3	X			16	Fix	High Current on VDDX During Reset
4	X			16	Fix	High Current on VDDX During Sleep
5	X			16	Fix	LCD State Machine Throughput Fails Using SDRAM at Full-Memory Clock Frequency
6	X			17	Fix	USB Stalls When More Than One USB Client Is Present
7	X			17	Fix	SDRAM Auto-Power-Up Failure
8	X			17	Fix	SDRAM RAS Precharge Counter May Not Work in the Presence of SMROM
9	X	X		17	Fix	DRAM Refresh Corrupting ROM/Flash Burst of 4/8 Timing
10	X	X	X	17	Eval	Data Contention Caused by Hardware, Software, or Watchdog Reset During SDRAM/SMROM Reads
11	X	X	X	18	Eval	Erroneous SMROM Precharge All (PALL) Command with Mode Register Set (MRS) Command After Hardware, Software, Watchdog, or Sleep Reset
12	X	X	X	19	Eval	UDC Not Responding to IN Packet After Receiving an SOF Packet

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	A0	B0	B1			
1	X	X	X	20	Eval	SDLC Feature
2	X	X	X	20	No Fix	SDLC Feature Not Supported

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	278240-001	22	Doc	Power Supply Voltages and Currents: Section 12.3
2	278240-001	22	Doc	SA-1110 Output Derating: Table 13-1
3	278240-001	23	Doc	Intel® StrongARM® SA-1110 Microprocessor: Section 1.1
4	278240-001	23	Doc	3.6864 MHz Option for GP[27] Alternate Output Function: Section 9.1.2.1
5	278240-001	23	Doc	Big and Little Endian: Section 3.1
6	278240-001	24	Doc	Static Memory Control Registers (MSC2 - 0): Section 10.2.4
7	278240-001	24	Doc	PCMCIA Overview: Section 10.6
8	278240-001	24	Doc	PPSR and PSDR Register Graphics: Section 11.13.4 and Section 11.13.6
9	278240-001	25	Doc	OS Timer Interrupt Enable Register: Section 9.4.5
10	278240-001	25	Doc	Big and Little Endian DMA Transfers: Figure 11-2
11	278240-001	26	Doc	Assignment of Signals and Serial Port Pins: Table 11-4 and Table 11-5
12	278240-001	27	Doc	Changes to Timing Diagrams
13	278240-001	42	Doc	DRAM Refresh Control Register (MDREFR): Section 10.2.2
14	278240-001	42	Doc	DRAM/SDRAM Self-Refresh in Sleep Mode: Section 10.4.7
15	278240-001	42	Doc	Hardware or Sleep Reset Procedures: Section 10.7.1
16	278240-001	42	Doc	Alternate Memory Bus Master Mode: Section 10.8
17	278240-001	42	Doc	Memory Bus Alternate Master: Section 16.8
18	278240-001	42	Doc	Test Unit Control Register (TUCR): Section D.1
19	278240-001	43	Doc	Power Manager GPIO Sleep State Register (PGSR): Section 9.5.7.7
20	278240-001	43	Doc	Variable Latency I/O Read Timing (Burst-of-Four, with One Wait Cycle Per Beat): Figure 10-16
21	278240-001	44	Doc	ROM Interface Overview: Section 10.5.1
22	278240-001	44	Doc	Overview of Operation: Section 10.1
23	278240-001	44	Doc	DRAM Refresh Control Register (MDREFR): Section 10.2.2.
24	278240-001	44	Doc	Hardware or Sleep Reset Procedures: Section 10.7.1
25	278240-001 278241-001	44	Doc	SA-1110 Tool Chains and Operating Systems Table
26	278240-001	44	Doc	Pin Operation in Sleep Mode: Section 9.5.6
27	278240-001	45	Doc	PPC Operation: Section 11.13.1
28	278240-001	45	Doc	PPC Sleep Mode Pin Direction Register: Section 11.13.6

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
29	278240-001	45	Doc	Variable Latency I/O Interface Overview: Section 10.5.5
30	278240-001	45	Doc	Software Dcache Flush: Section 6.2.3
31	278240-001	45	Doc	Sleep Mode: Section 9.5.3
32	278240-001	45	Doc	SA-1110 AC Timing Table - Memory Bus: Table 13-2.
33	278240-001	46	Doc	UDC Register Definitions: Section 11.8.2
34	278240-001	46	Doc	Valid Settings for the DDARn Register: Table 11-6
35	278240-001	46	Doc	GPIO Alternate Functions Table: Section 9.1.2
36	278240-001	46	Doc	Intel® StrongARM®SA-1110 Boundary-Scan (BS) Register: Section 16.6.3
37	278240-001	47	Doc	Boundary-Scan Signals and Pins: Table 16-2
38	278240-001	50	Doc	GPIO Alternate Functions: Section 9.1.2
39	278240-001	50	Doc	UART Data Register: Section 11.11.6
40	278240-001	50	Doc	Reset Controller Status Register: Section 9.6.1.2
41	278240-001	50	Doc	Reset Interrupt Mask: Section 11.8.3.8
42	278240-001	51	Doc	Address Field: Section 11.10.2.3
43	278240-001	51	Doc	Pin State During Sleep: Table 9-3
44	278240-001	51	Doc	Alternate Memory Bus Master Mode: Section 10.8
45	278240-001	51	Doc	Exiting Idle Mode: Section 9.5.2.2
46	278240-001	51	Doc	Module Considerations: Section 13.2
47	278240-001	51	Doc	Register 0 – ID: Section 5.2.1
48	278240-001	52	Doc	SA-1110 AC Timing Table - Memory Bus: Table 13-2
49	278240-001	52	Doc	Aborts and Nonexistent Memory: Section 10.1.7
50	278240-001	52	Doc	DRAM Configuration Register (MDCNFG): Section 10.2.1
51	278240-001	52	Doc	DRAM Refresh Control Register (MDREFR): Section 10.2.2
52	278240-001	53	Doc	CAS Waveform Rotate Registers (MDCAS00, MDCAS01, MDCAS02, MDCAS20, MDCAS21, MDCAS22): Section 10.2.3
53	278240-001	53	Doc	Static Memory Control Registers (MSC2-0): Section 10.2.4
54	278240-001	53	Doc	Expansion Memory (PCMCIA) Configuration Register (MECR): Section 10.2.5
55	278240-001	53	Doc	SMROM Configuration Register (SMCNFG): Section 10.3
56	278240-001	54	Doc	DRAM/SDRAM Refresh: Section 10.4.6
57	278240-001	54	Doc	ROM Interface Overview: Section 10.5.1
58	278240-001	54	Doc	SMROM State Machine: Section 10.5.11
59	278240-001	54	Doc	Memory Interface Reset and Initialization: Section 10.7
60	278240-001	55	Doc	Hardware or Sleep Reset Procedures: Section 10.7.1

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
61	278240-001	55	Doc	Software or Watchdog Reset Procedures: Section 10.7.2
62	278240-001	55	Doc	Timing Parameters: Section 13.6
63	278240-001	55	Doc	FLASH Memory Timing Diagrams and Parameters: Section 10.5.8
64	278240-002	55	Doc	Exiting Idle Mode: Section 9.5.2.2
65	278240-002	56	Doc	Register Summary: Appendix A

Identification Information

Ordering Information

GDS1110AB SL3Z4 and GDS1110BB SL3Z5.

This document contains errata for the B1 stepping of the SA-1110 Microprocessor. The SA-1110 device revision that is affected by this errata can be identified as ordering numbers GDS1110AB SL3Z4 and GDS1110BB SL3Z5.

Ordering Numbers	Speed (MHz)	Voltage (V)	Package
GDS1110AB SL3Z4	133	1.55	mBGA
GDS1110BB SL3Z5	206	1.75	mBGA

Related Information

None for this revision of this specification update.

Errata

1. Incorrect Sign-Extended Value in Register After a Read Buffer Allocate

Problem: After a read buffer allocate, a Load Register Signed Halfword (LDRSH) or a Load Register Signed Byte (LDRSB) will not return the correct value in the register, due to long propagation delays in the sign extend logic.

Workaround: Execute the command twice and the data is guaranteed to be correctly sign extended for the second read.

Status: No Fix

2. LCD Ghost Lines

Problem: The SA-1110 LCD when driving a color passive display has diagonal ghost lines and flicker. These ghost lines are image dependent and are more evident with intensities 3 and 11.

Workaround: None. There is a marked improvement by setting bits 11:10 in LCD Control Register 0 (Address 0h B010 0000) to 0x8. The actual setting of bits 11:10 should be experimented with to determine the best LCD performance.

Status: No Fix

3. High Current on VDDX During Reset

Problem: The SA-1110 exhibits high VDDX current under the scenario of power-on reset and hardware reset with subsequent VDD failure.

Workaround: Use external logic to ensure that VDD powers up with VDDX and cannot be held low when hardware reset is asserted. In a typical application, this would require that VDD be enabled if either PWR_EN = 1 or nRESET = 0.

Status: Fix

4. High Current on VDDX During Sleep

Problem: The SA-1110 exhibits high VDDX current (2.5 mA) during sleep.

Workaround: None identified.

Status: Fix

5. LCD State Machine Throughput Fails Using SDRAM at Full-Memory Clock Frequency

Problem: The LCD controller fails when the frame buffer is read from SDRAM that does burst transfers at the full-memory clock frequency (one-half CPU frequency). When using other memory types, which cannot burst at full-memory clock frequency, or using SDRAM at half-memory clock frequency (one-fourth CPU frequency), the LCD controller works correctly.

Workaround: Set up SDRAM used for the LCD frame buffer to run at half-memory clock frequency.

Status: Fix

6. USB Stalls When More Than One USB Client Is Present

Problem: When multiple USB clients are present, the USB stalls after the master completes a transmission to another device. The USB does not respond when the master addresses it.

Workaround: Do not allow multiple clients on the USB bus.

Status: Fix

7. SDRAM Auto-Power-Up Failure

Problem: If the memory controller is configured to allow SDRAM auto-power-down of minimum possible duration (SDCKE 1 low for exactly one and one-half memory clocks), the subsequent auto-power-up (SDCKE 1 goes high and appropriate SDCLK 2:1 starts running) may not work correctly.

Workaround: For SDRAM transfers, increase RAS precharge time (MDCNFG:TRP2 or MDCNFG:TRP0) to be greater than or equal to 5. This forces the first SDRAM transfer following auto-power-up to be delayed, such that SDCKE 1 can be sampled high upon a rising edge of SDCLK 2:1 prior to sampling the next ACT command.

Status: Fix

8. SDRAM RAS Precharge Counter May Not Work in the Presence of SMROM

Problem: Because SMROM does not require the use of the SA-1110's counter for minimum SDRAM RAS precharge time, this counter is overridden during SMROM transfers. The override logic does not consistently use upper address bits to distinguish between SDRAM and SMROM. Therefore, when like-numbered SMROM and SDRAM chip selects (for example, nCS 0 and nRAS/nSDCS 0) are enabled, the RAS precharge counter may not work for those SDRAM chip selects.

Workaround: Avoid enabling like-numbered chip selects for SMROM and SDRAM. For example, enable SMROM only on nCS 1:0 and SDRAM only on nRAS/nSDCS 3:2.

Status: Fix

9. DRAM Refresh Corrupting ROM/Flash Burst of 4/8 Timing

Problem: Asynchronous DRAM and SDRAM refreshes are allowed to interrupt burst transfers to any static, asynchronous memory type (ROM, SRAM, VLIO, or Flash) between 32-bit transfers. This works properly when any of those memory types are configured for non-burst timings (MCSx:RTx = 0 or 1). But when ROM/Flash is configured for burst timings (MSCx:RTx = 2 or 3), burst-of-4/8 aligned addresses may erroneously use the burst access time (MCSx:RDNx) rather than the intended non-burst access time (MSCx:RDFx). This happens whenever the refresh request (internally generated) occurs just prior to a burst-of-4/8 unaligned address. The problem will affect burst-of-4 timings on either 16-bit or 32-bit data busses, or burst-of-8 timings on 16-bit busses.

Workaround: Use non-burst timing (MSCx:RTx = 0) for ROM/Flash.

Status: Fix

10. Data Contention Caused by Hardware, Software, or Watchdog Reset During SDRAM/SMROM Reads

Problem: If a SA-1110 hardware, software, or watchdog reset occurs while SDRAM/SMROM is executing a read command, the SA-1110 will de-assert all control pins: SDCKE 1:0, SDCLK 2:0, nCS 3:0, nRAS/nSDCS 3:0, nSDRAS, nSDCAS, nWE, nOE, and nCAS/DQM 3:0. This correctly prevents new commands from being started. But, because SDCKE 1:0 and SDCLK 2:0 are de-asserted within a few cycles of the last read command, that read may not get finished. Instead, SDRAM/SMROM may continue to drive D 31:0 during reset assertion and after reset de-assertion: until a few cycles after SDCKE 1:0 and SDCLK 2:0 are asserted again and the final read data has

been driven. This continuous D 31:0 drive by SDRAM/SMROM may contend with read data from other memory devices or write data from the SA-1110 itself.

Workarounds (2) for Hardware Reset: Use the following workarounds for a hardware reset:

1. Do not use hardware reset after the initial power-on hardware reset.
2. During each assertion of the SA-1110's hardware reset pin (nRESET=0), temporarily remove power from SDRAM/SMROM VDD and VDDQ pins.

Workaround for Software Reset: Prior to executing a software reset, all outstanding SDRAM and SMROM transfers must be allowed to complete and the banks must be disabled via writes to the MDCNFG and SMCNFG registers.

1. If burst reads from SMROM are not already enabled, enable them without changing the number of row address bits, CAS latency, or RAS latency.
   a. Write MDCAS00, MDCAS01, and MDCAS02 with their present number of leads 1's, but filled through the 96th bit with the 2-bit repeating pattern of "0" followed by "1" (see Section 10.2.3.2 for explanation).
   b. Force a mode register set (MRS) command by writing SMCNFG with its present value. The MRS configures the SMROMs' internal mode registers for a burst length of eight.
2. If the instruction cache is not already enabled, enable it by setting bit 12 of the coprocessor 15 control register (see Chapter 5 and Chapter 6). This causes subsequent fetches to be performed as 8-word bursts.
3. Align the store instruction which alters SMCNFG to an 8-word address boundary. Locate the store instructions that alter MDCNFG and RSRR at the subsequent two addresses. Aligning these three instructions to the start of a cache line ensures that they are fetched together and executed prior to any other SMROM read.

Workaround for Watchdog Reset: Do not use watchdog reset. The combination of watchdog interrupt and software reset may be used instead of watchdog reset.

Status: Eval

11. Erroneous SMROM Precharge All (PALL) Command with Mode Register Set (MRS) Command After Hardware, Software, Watchdog, or Sleep Reset

Problem: After any type of reset (hardware, software, watchdog, or sleep), an SMROM mode register set (MRS) command may be followed in less than three SDCLK cycles by an unnecessary SMROM precharge all (PALL) command. According to SMROM specifications, a minimum of three cycles is required between issue of MRS and any subsequent command. Issue of the unnecessary PALL command is dependent upon the precise timing of reset within the SDCLK cycle, and upon use of MDREFR:K0DB2=1.

Workaround: Confirm that SMROM are insensitive to the issue of unnecessary PALL commands that follow MRS commands by less than three SDCLK cycles.

Status: Eval

12. UDC Not Responding to IN Packet After Receiving an SOF Packet

Problem: The host will request data from the UDC by sending an IN packet to Endpoint 2. The UDC must respond with a NAK signal if it does not currently have any data stored in the FIFO. Sporadically, the UDC will not respond with a NAK signal after an SOF packet has been received.

Workaround: Connect a USB hub between the UDC and the host system.

Status: Eval

Specification Changes

1. SDLC Feature

The SDLC feature is not available in this release of the product.

2. SDLC Feature Not Supported

Effective January 2000, the SDLC feature is not supported by the SA-1110 device.

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

1. Power Supply Voltages and Currents: Section 12.3

Values need to be added for the following table.

Table 12-3. SA-1110 Power Supply Voltages and Currents

Parameter	SA-1110		Units
	AB	BB	
Maximum operating frequency	133	206	MHz
Maximum run mode power (total VDD + VDDX)	TBD	TBD	mW
Typical run mode power (total VDD + VDDX)	240	400	mW
Maximum idle mode power† (total VDD + VDDX)	TBD	TBD	mW
Typical idle mode power† (total VDD + VDDX)	75	100	mW
Maximum sleep mode current † (total VDD + VDDX)	65	75	uA
Typical sleep mode current † (total VDD + VDDX)	40	50	uA
VDD			
Minimum internal power supply voltage	1.47	1.58	V
Nominal internal power supply voltage	1.55	1.75	V
Maximum internal power supply voltage	1.63	1.93	V
VDDX			
Minimum external power supply voltage	3.00	3.00	V
Nominal external power supply voltage	3.30	3.30	V
Maximum external power supply voltage	3.60	3.60	V

† Room temperature specification.

2. SA-1110 Output Derating: Table 13-1

Values need to be added for the following table.

Output Signal	Load for Nominal Value	Output Derating (ns/pF) VDD = 1.55 V rising edge	Output Derating (ns/pF) VDD = 1.55 V falling edge	Output Derating (ns/pF) VDD = 1.75 V rising edge	Output Derating (ns/pF) VDD = 1.75 V falling edge	Note
All outputs	50 pF	tbd	tbd	tbd	tbd	1

NOTE:
1. Parameter verified by design

3. Intel® StrongARM® SA-1110 Microprocessor: Section 1.1

The next-to-last sentence in second paragraph changed from “The nonshaded boxes are new or updated features for the SA-1110.” to “The nonshaded boxes are new or updated features for the SA-1110; most of these features are equivalent to that of the SA-1100.”

Table 1-2 caption changed from *Changes to the SA-1110 Core* to *Changes to the SA-1110 Core from the SA-110*. Table 1-3 caption changed from *Additional Features Built into SA-1110 Chipset* to *Feature Additions to the SA-1110 from the SA-110*. A *Feature Additions to the SA-1110 from the SA-1100* table added:

- Synchronous DRAM (SDRAM) support
- Synchronous mask ROM (SMROM) support (32-bit only) on CS0-3
- Ready input signal for variable latency I/O devices (for example, graphics chips)
- CS4 and CS5 for variable latency I/O devices, ROM, or Flash memory
- CS3 support for variable latency I/O devices (instead of SRAM)
- Support for burst (page-mode) read timings from Flash memory
- Support for 16-bit data busses on all memory types (except SMROM)
- Support for SRAM, DRAM, and SDRAM in the same system

4. 3.6864 MHz Option for GP[27] Alternate Output Function: Section 9.1.2.1

The following section added:

“When GP[27] is configured for its alternate output function by setting bit 27 in both the GAFR and GPDR, bit 29 of the test unit control register (TUCR) at physical address 0x9003 0008 can be set to select the 3.6864 MHz oscillator output instead of the 32.768 KHz oscillator output. When TUCR[29] is cleared the 32.768 KHz oscillator output is selected again. Neither option provides a fixed phase relationship with any other pin signals; and some glitching may occur when switching between the two options.

The 3.6864 MHz option is particularly useful for companion chips that require some clock cycles after assertion of VDD_FAULT or BATT_FAULT. The oscillator output will continue through the first step of the sleep shutdown sequence, which lasts for one cycle of the power manager’s 32.768 KHz clock (~30 microseconds). Thus, at least 112 cycles of 3.6864 MHz oscillation are provided prior to shutdown. See Section 9.5.3 for a detailed description of sleep mode and the sleep shutdown sequence.”

5. Big and Little Endian: Section 3.1

Last sentence in fourth paragraph changed from “Instruction fetches and word load and stores are not changed by the state of the big endian bit.” to “Instruction fetches and word load and stores are not changed by the state of the big endian bit, except when those accesses are performed with memory on 16-bit data busses. See Chapter 10 for details on configuring data bus widths for various memory types.”

6. Static Memory Control Registers (MSC2 - 0): Section 10.2.4

Description of bit 2 in the register bit table changed to:

Bit	Name	Description
2	RBWx	ROM bus width. 0 – 32 bits 1 – 16 bits On reset, the RBW0 field in MSC0 is loaded with the inverse of the ROM_SEL pin. It can be subsequently overwritten. RBWx bits must remain clear if the corresponding chip selects are configured for Synchronous Mask ROM (SMROM). Also, if nCS<0> is configured for SMROM by holding the SMROM_EN pin high during reset, the ROM_SEL pin must be held high. See Section 10.3 for details on SMROM configuration.

7. PCMCIA Overview: Section 10.6

Third sentence in the third paragraph changed from “When nPCE1 is low, A<0> is ignored and an odd byte is transferred across D<15:8>. “ to “When nPCE2 is low, A<0> is ignored and an odd byte is transferred across D<15:8>. “

8. PPSR and PSDR Register Graphics: Section 11.13.4 and Section 11.13.6

The PPSR register graphic drawing is replaced with:

Address: 0h 9006 0004 — **PPSR: PPC Pin State Register** — **Read/Write**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved										SFRM	SCLK	RXD4	TXD4	RXD3	TXD3
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RXD2	TXD2	RXD1	TXD1	L_ BIAS	L_ FCK	L_ LCK	L_ PCK	LDD <7>	LDD <6>	LDD <5>	LDD <4>	LDD <3>	LDD <2>	LDD <1>	LDD <0>
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The PSDR register graphic drawing is replaced with:

Address: 0h 9006 000C — **PSDR: PPC Sleep Mode Direction Register** — **Read/Write**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved										SFRM	SCLK	RXD4	TXD4	RXD3	TXD3
Hard Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RXD 2	TXD2	RXD1	TXD1	L_ BIAS	L_ FCLK	L_ LCLK	L_ PCLK	LDD <7>	LDD <6>	LDD <5>	LDD <4>	LDD <3>	LDD <2>	LDD <1>	LDD <0>
Hard Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

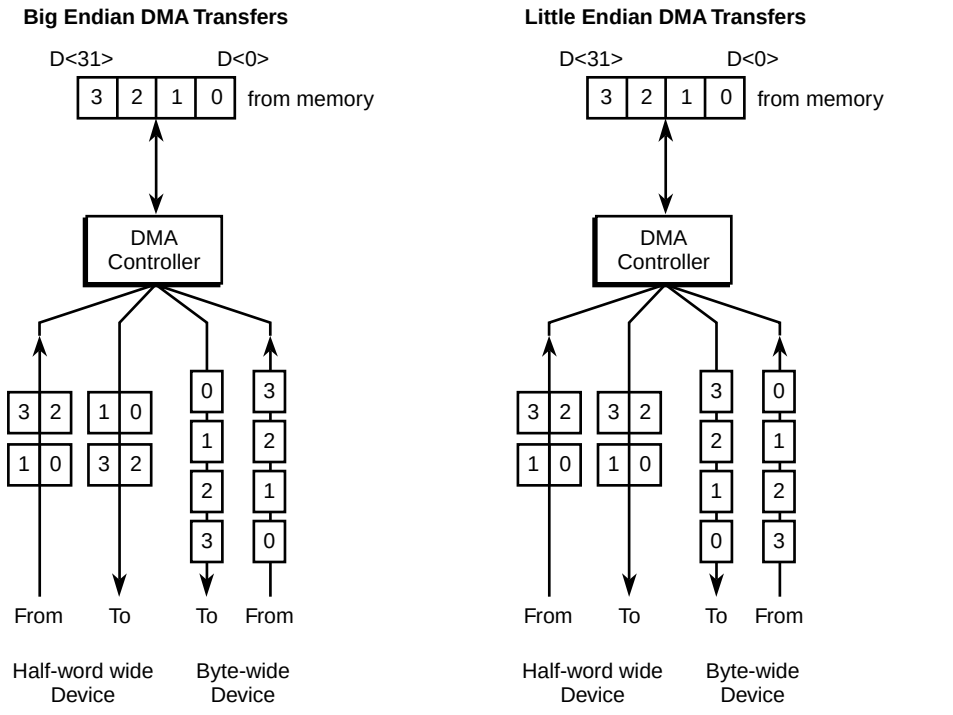
9. OS Timer Interrupt Enable Register: Section 9.4.5

The description of the OS Timer Interrupt Enable Register changed to:

Bit	Name	Description
0	E0	Interrupt enable channel 0. This bit is set by software and allows a match between match register 0 and the OS timer to assert interrupt bit M0 in the OSSR.
1	E1	Interrupt enable channel 1. This bit is set by software and allows a match between match register OSMR[1] and the OS timer to assert interrupt bit M1 in the OSSR.
2	E2	Interrupt enable channel 2. This bit is set by software and allows a match between match register OSMR[2] and the OS timer to assert interrupt bit M2 in the OSSR.
3	E3	Interrupt enable channel 3. This bit is set by software and allows a match between match register OSMR[3] and the OS timer to assert interrupt bit M3 in the OSSR.
31...4	—	Reserved.

10. Big and Little Endian DMA Transfers: Figure 11-2

Figure 11-2 replaced with:



11. Assignment of Signals and Serial Port Pins: Table 11-4 and Table 11-5

Table 11-4 “Dedicated Peripheral Pins” changed to:

Peripheral	GPIO Pin	Function
LCD Controller	L_PCLK	Pixel clock
	L_LCLK	Line clock/horizontal sync pulse
	L_FCLK	Frame clock/vertical sync pulse
	L_BIAS	A/C bias signal
	LDD<7:0>	Pixel data
Serial port 0: USB	UDC+	Positive differential receiver
	UDC-	Negative differential receiver
Serial port 1: SDLC/UART	TXD_1	Serial transmit data
	RXD_1	Serial receive data
Serial port 2: ICP	TXD_2	Serial transmit data
	RXD_2	Serial receive data
Serial port 3: UART	TXD_3	Serial transmit data
	RXD_3	Serial receive data
Serial port 4: MPC/SSP	TXD_C	Serial transmit data
	RXD_C	Serial receive data
	SCLK_C	Serial clock
	SFRM_C	Serial frame clock

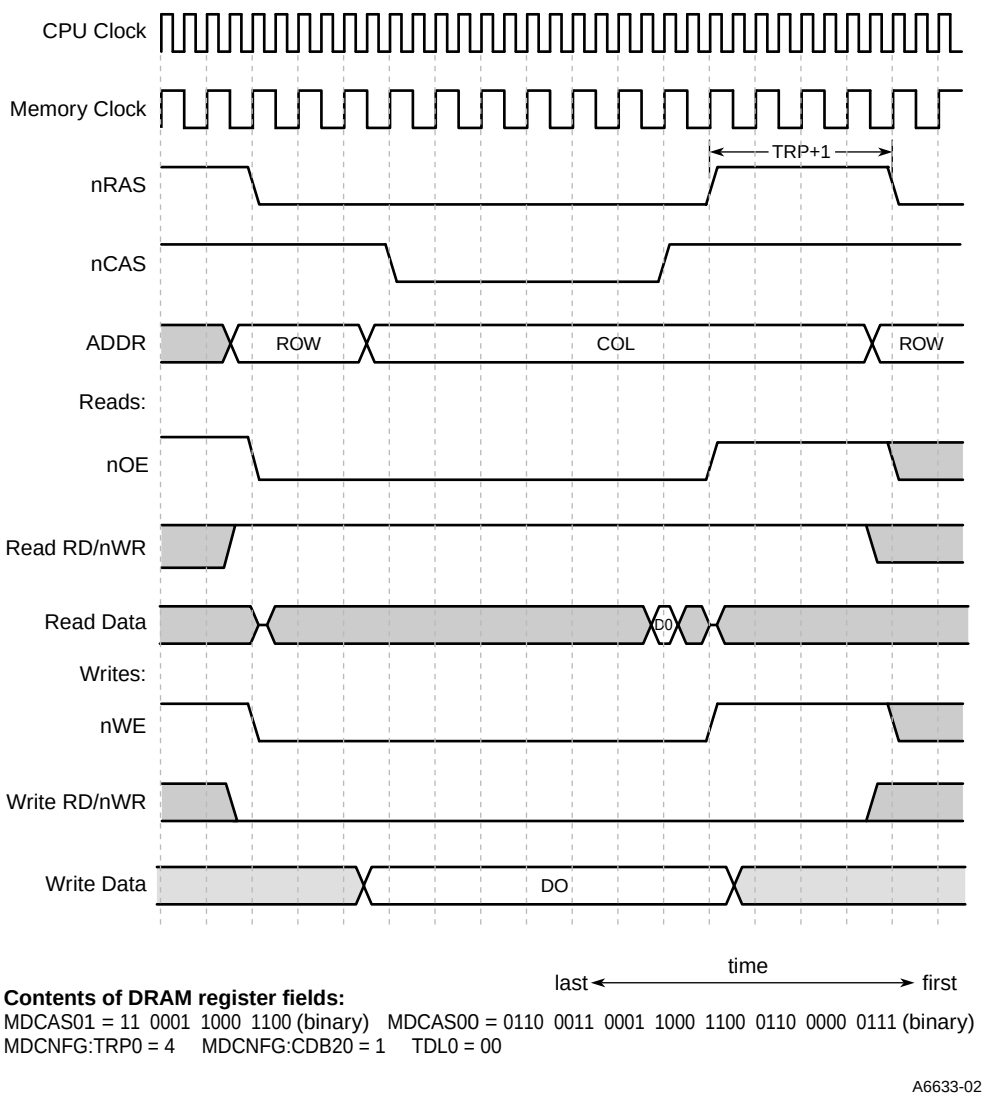
Table 11-5 “Peripheral Unit GPIO Pin Assignment” changed to:

Peripheral	GPIO Pin	Function
LCD Controller	GPIO<2>	LDD<8> pin for dual-panel color mode.
	GPIO<3>	LDD<9> pin for dual-panel color mode.
	GPIO<4>	LDD<10> pin for dual-panel color mode.
	GPIO<5>	LDD<11> pin for dual-panel color mode.
	GPIO<6>	LDD<12> pin for dual-panel color mode.
	GPIO<7>	LDD<13> pin for dual-panel color mode.
	GPIO<8>	LDD<14> pin for dual-panel color mode.
	GPIO<9>	LDD<15> pin for dual-panel color mode.
Serial port 0: USB	N/A	None.
Serial port 1: SDLC/UART	GPIO<14>	Transmit pin for UART when SDLC and UART both needed.
	GPIO<15>	Receive pin for UART when SDLC and UART both needed.
	GPIO<16>	Sample clock input/output to SDLC.
	GPIO<17>	Toggle to drive external tristate for SDLC transmit packets.
	GPIO<18>	Sample clock input to UART.
Serial port 2: ICP	N/A	None.
Serial port 3: UART	GPIO<20>	Sample clock input to UART.
Serial port 4: MPC/SSP	GPIO<10>	Transmit pin for SSP when MCP and SSP both needed.
	GPIO<11>	Receive pin for SSP when MCP and SSP both needed.
	GPIO<12>	Serial clock pin for SSP when MCP and SSP both needed.
	GPIO<13>	Serial frame clock pin for SSP when MCP and SSP both needed.
	GPIO<19>	Clock input pin for SSP to drive the frame and sample rates when other than nonmultiple of 3.6864 MHz needed.
	GPIO<21>	Clock input pin for MCP to drive the frame and sample rates when other than 12 Mbps needed.

12. Changes to Timing Diagrams

Design changes to the RD/nWR pin affected changes to the following timing diagrams:

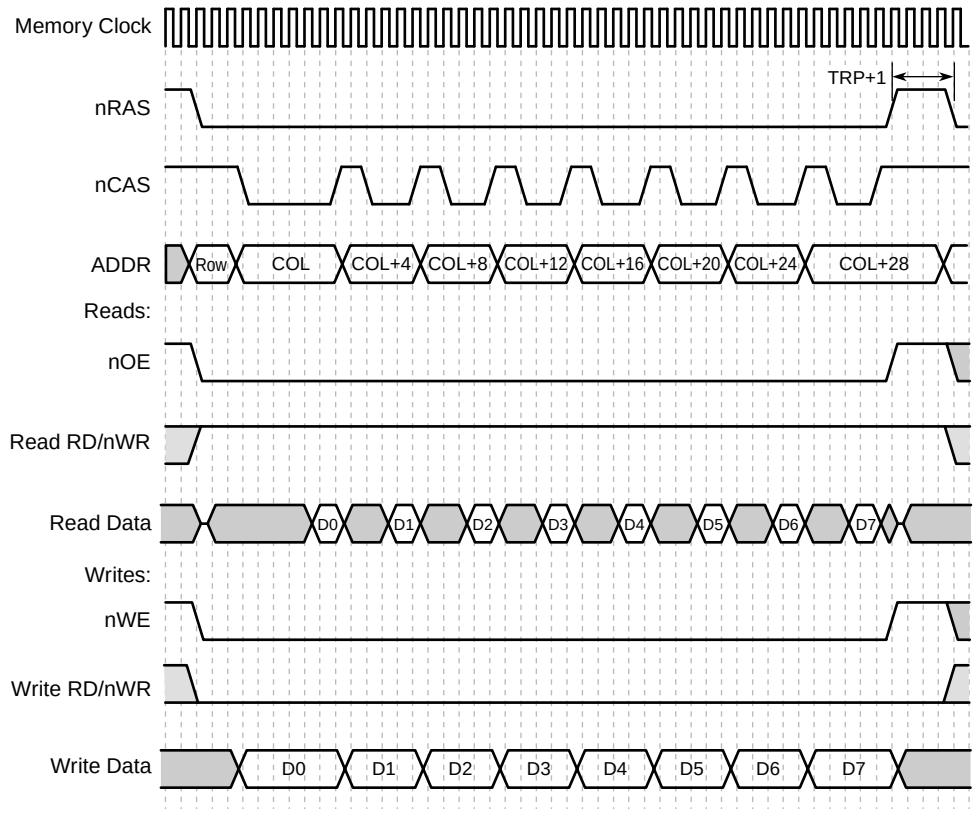
Figure 10-5: DRAM Single-Beat Transactions



Contents of DRAM register fields:
MDCAS01 = 11 0001 1000 1100 (binary) MDCAS00 = 0110 0011 0001 1000 1100 0110 0000 0111 (binary)
MDCNFG:TRP0 = 4 MDCNFG:CDB20 = 1 TDL0 = 00

A6633-02

Figure 10-6: DRAM Burst-of-Eight Transactions



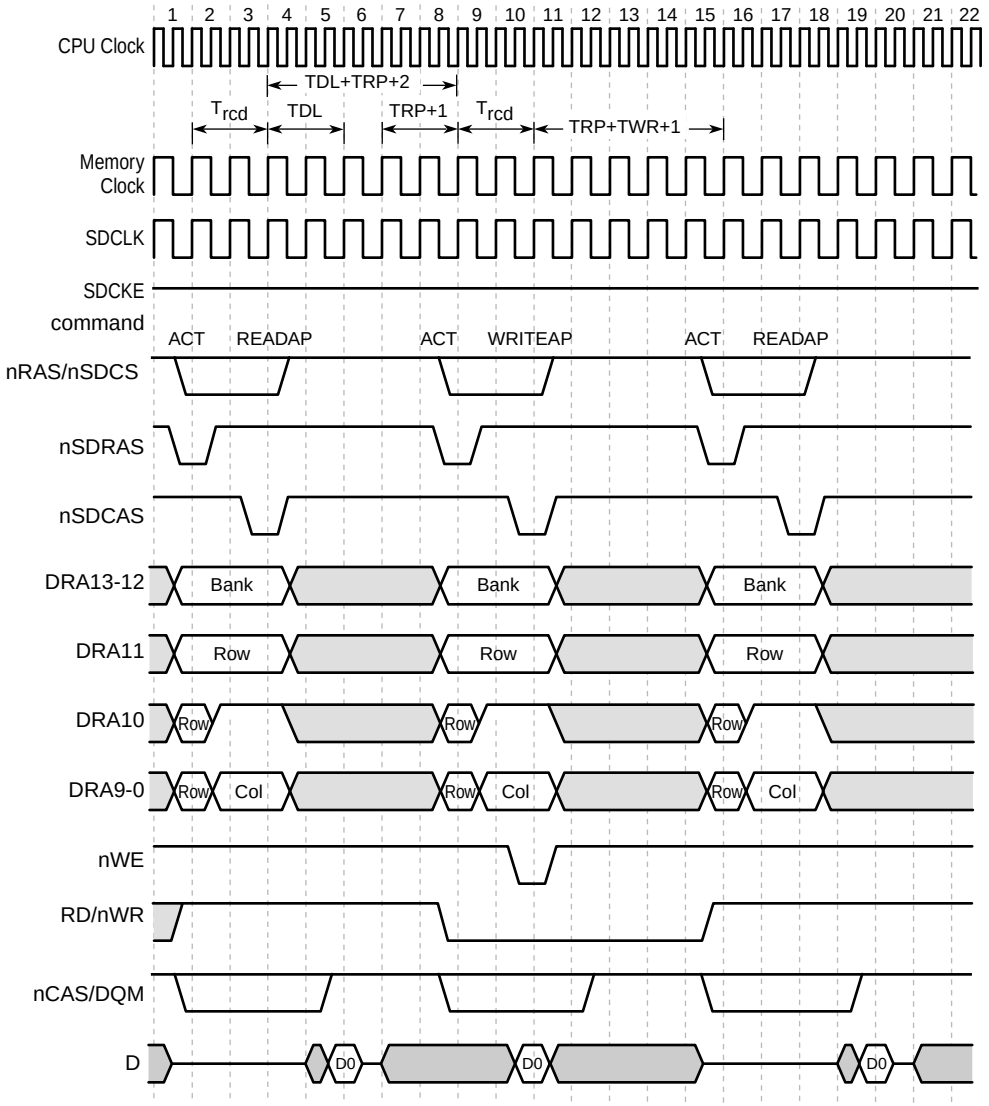
Contents of DRAM register fields:

MDCAS01 = 11 0001 1000 1100 (binary) MDCAS00 = 0110 0011 0001 1000 1100 0110 0000 0111 (binary)

MDCNFG: TRP0 = 4 MDCNFG: CDB20 = 1 TDL0 = 00

A6634-02

Figure 10-8: SDRAM 1-Beat Read/Write/Read Timing for 4 Bank x 4 M x 4 Bit Organization (64 Mbit)



Contents of DRAM register fields:

MDCNFG:DTIM0=1 MDCNFG:DWID0=0 MDCAS00=0101 0101 0101 0101 0101 0101 0101 0111(binary)
MDCNFG:DRAC0=5 MDCNFG:CDB20=0 MDCNFG:TRP0=1 MDCNGF:TDL0=2 MDCNFG:TWR0=3

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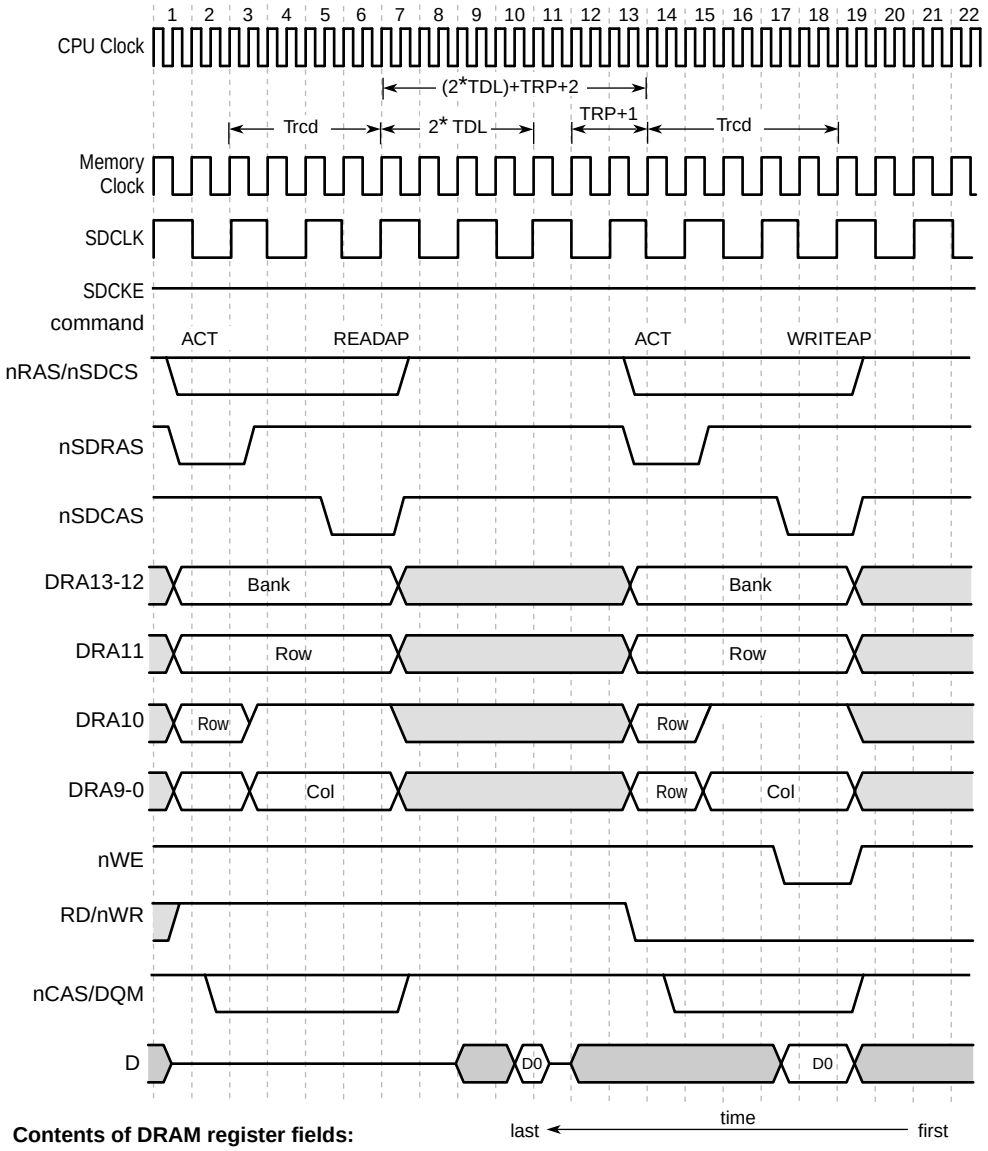
Figure 10-9: SDRAM 1-Beat Read/Write Timing for 4 Bank x 4 M x 4 Bit Organization (64 Mbit) at Half Memory Clock Frequency (MDREFR:KnDB2=1)**)**



Contents of DRAM register fields:

MDCNFG:DTIM0=1 MDCNFG:DWID0=0 MDCAS00=0101 0101 0101 0101 0101 0101 0111 1111(binary)
MDCNFG:DRAC0=5 MDCNFG:CDB20=0 MDCNFG:TRP0=1 MDCNGF:TDL0=2 MDCNFG:TWR0=3

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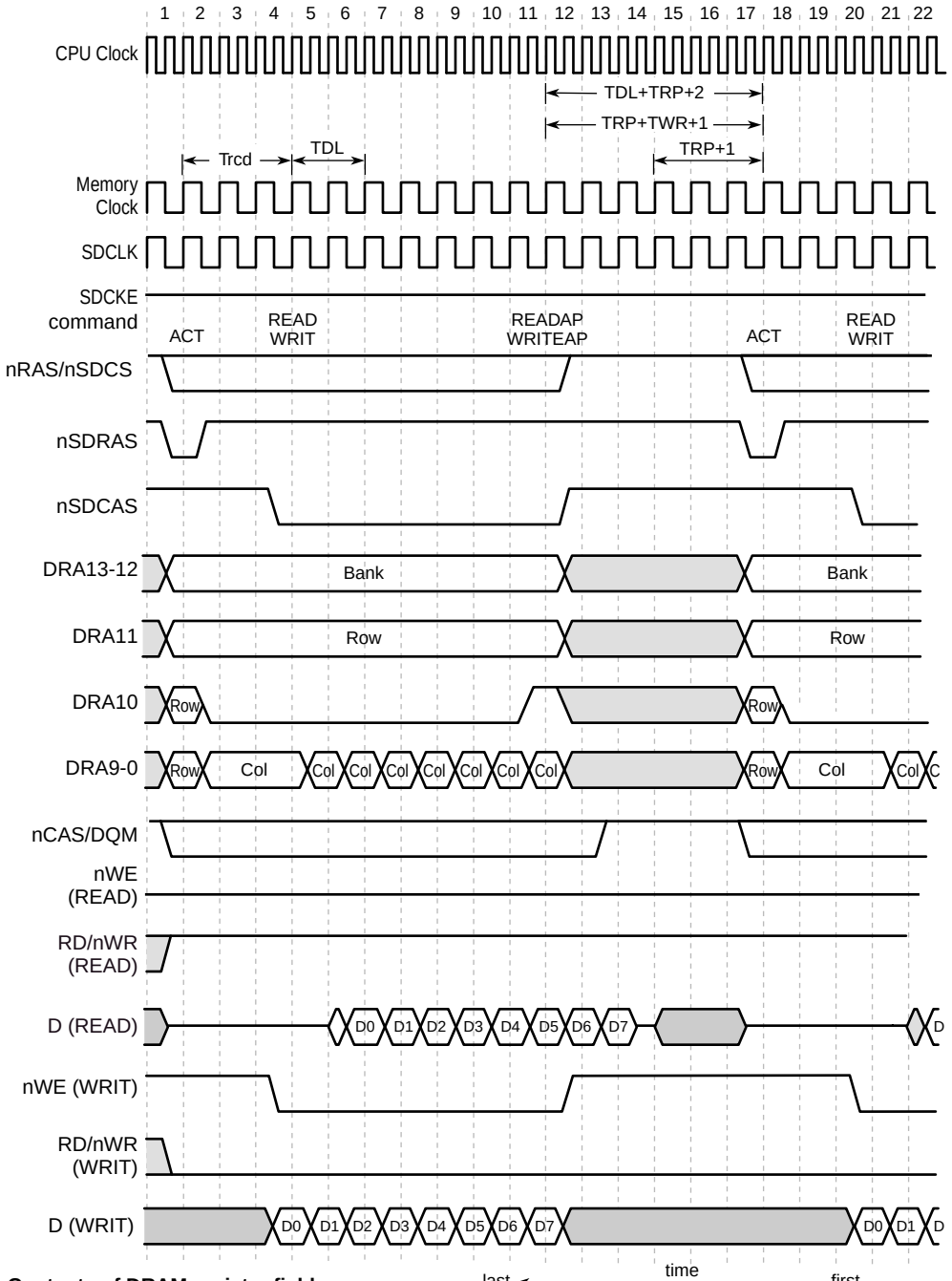
Figure 10-10: SDRAM 8-Beat Read/Write Timing for 4 Bank x 4 M x 4 Bit Organization (64 Mbit)

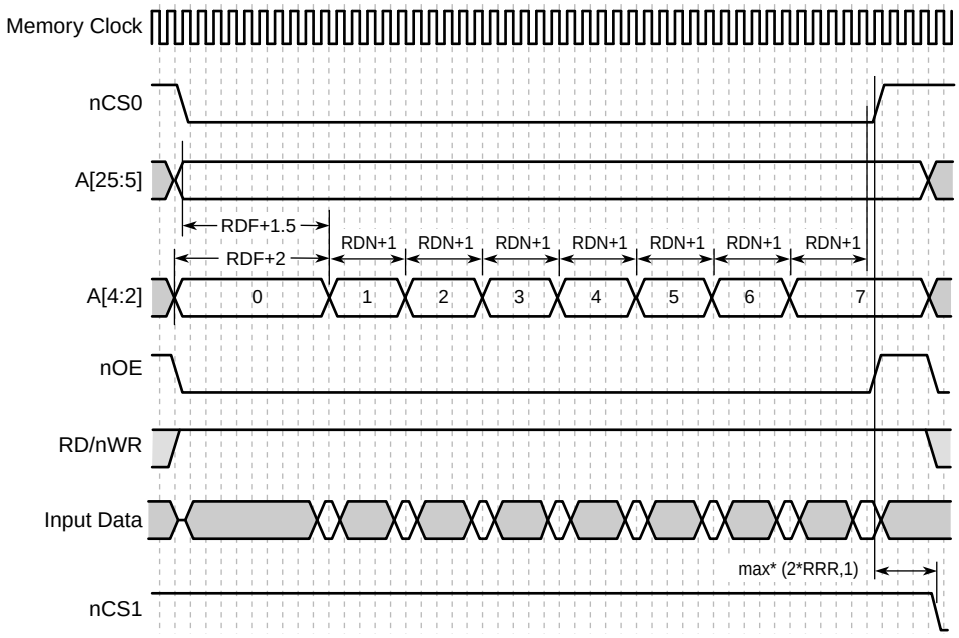


Contents of DRAM register fields:

MDCNFG:DTIM0=1 MDCNFG:DWID0=0 MDCAS00=0101 0101 0101 0101 0101 0101 0101 1111(binary)
MDCNFG:DRAC0=5 MDCNFG:CDB20=0 MDCNFG:TRP0=2 MDCNGF:TDL0=2 MDCNFG:TWR0=3

A6637-02

Figure 10-12: Burst-of-Eight ROM or Flash Read Timing Diagram



Contents of static memory register fields:

MSC0:RDF0=8 MSC0:RDN0=4 MSC0:RRR0=2

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Figure 10-13: Eight-Beat Burst Read from Burst-of-Four ROM or Flash

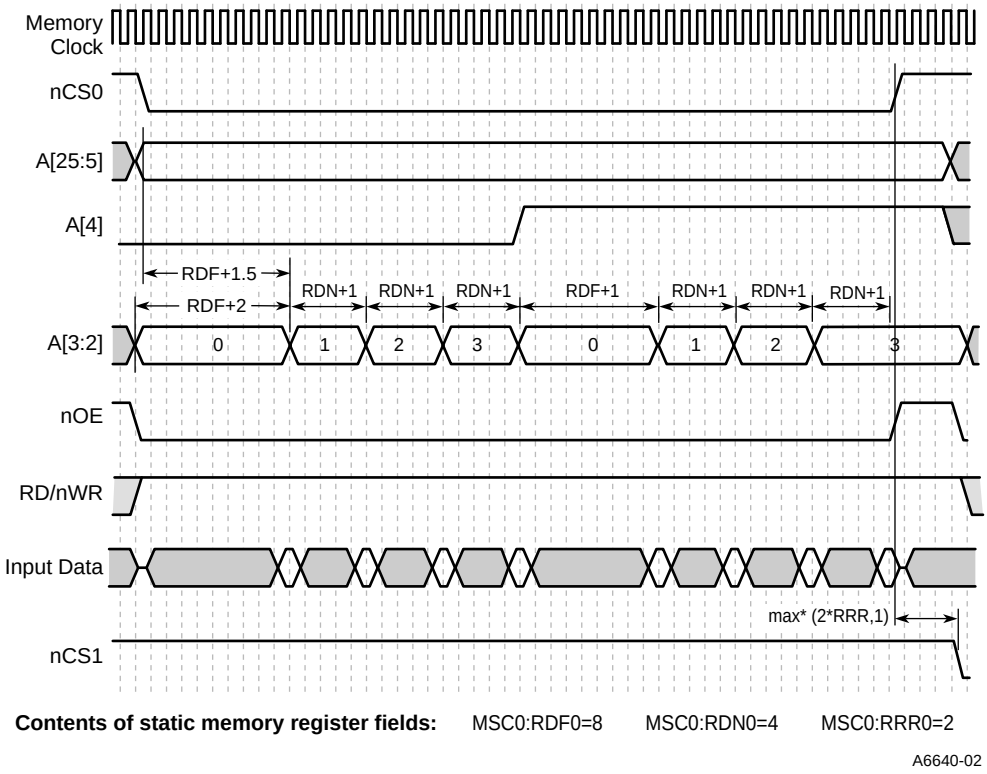
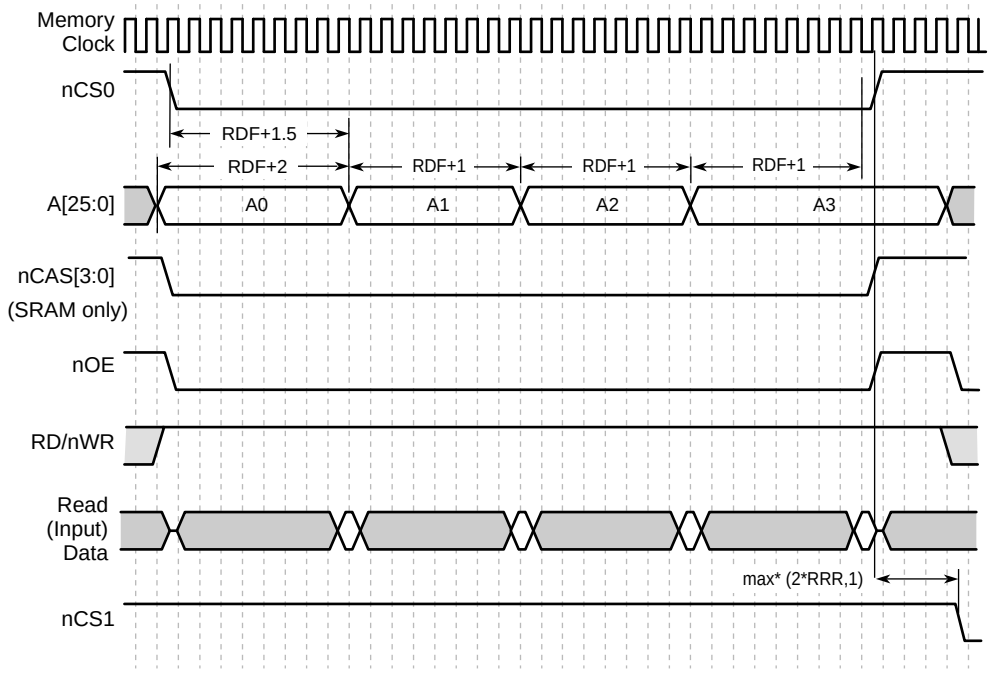


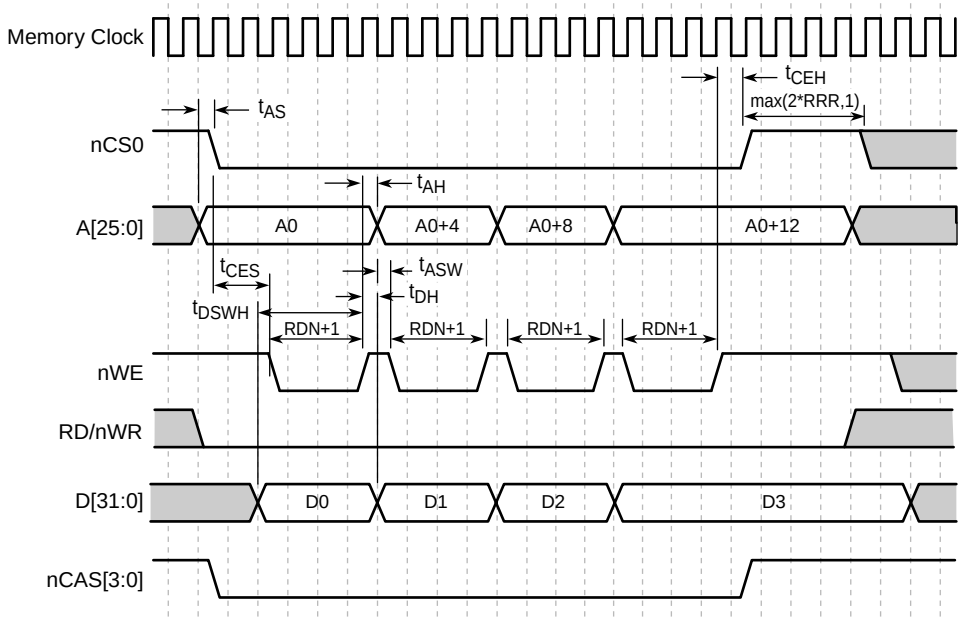
Figure 10-14: Nonburst ROM, SRAM, or Flash Read Timing Diagram — Four Data Beats



Contents of static memory register fields: MSC0:RDF0=7 MSC0:RRR0=2

A6641-02

Figure 10-15: SRAM Write Timing Diagram (4-Beat Burst)



Contents of static memory register fields: MSC0: RDN0=2 MSC0:RRR0=2

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Figure 10-16: Variable Latency I/O Read Timing (Burst-of-Four, with One Wait Cycle Per Beat)

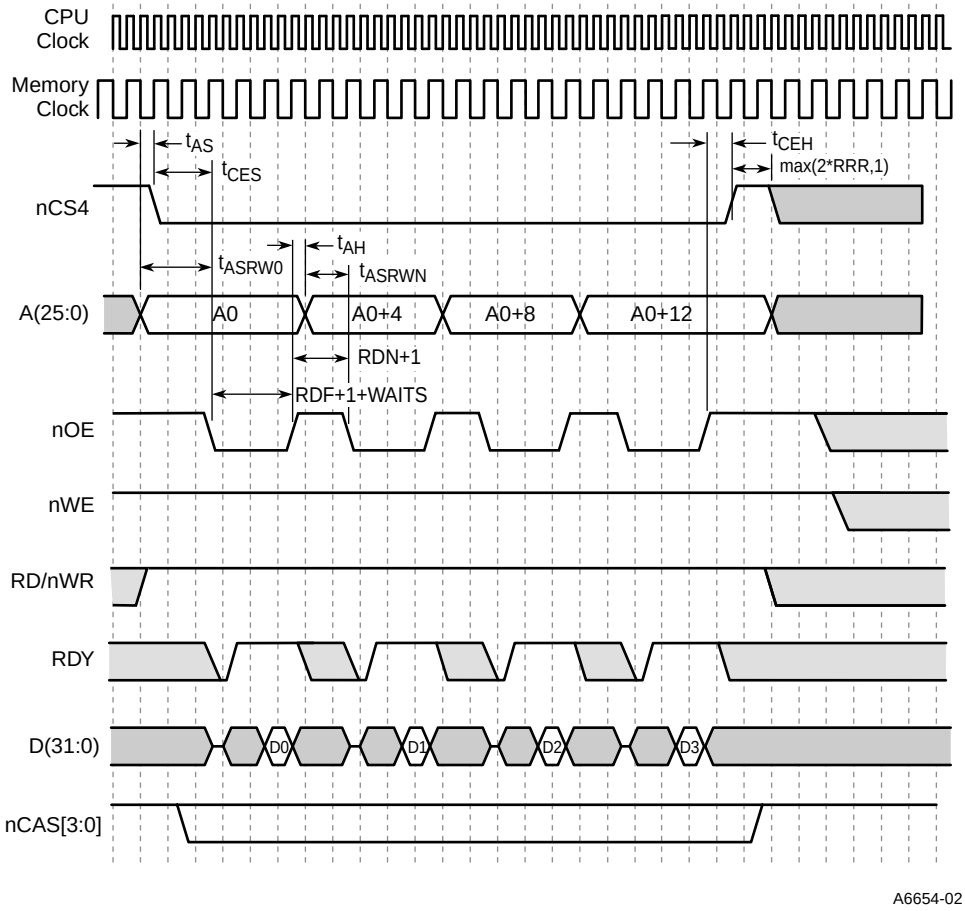


Figure 10-17: Variable Latency I/O Write Timing (Burst-of-Four, with One Wait Cycle Per Beat)

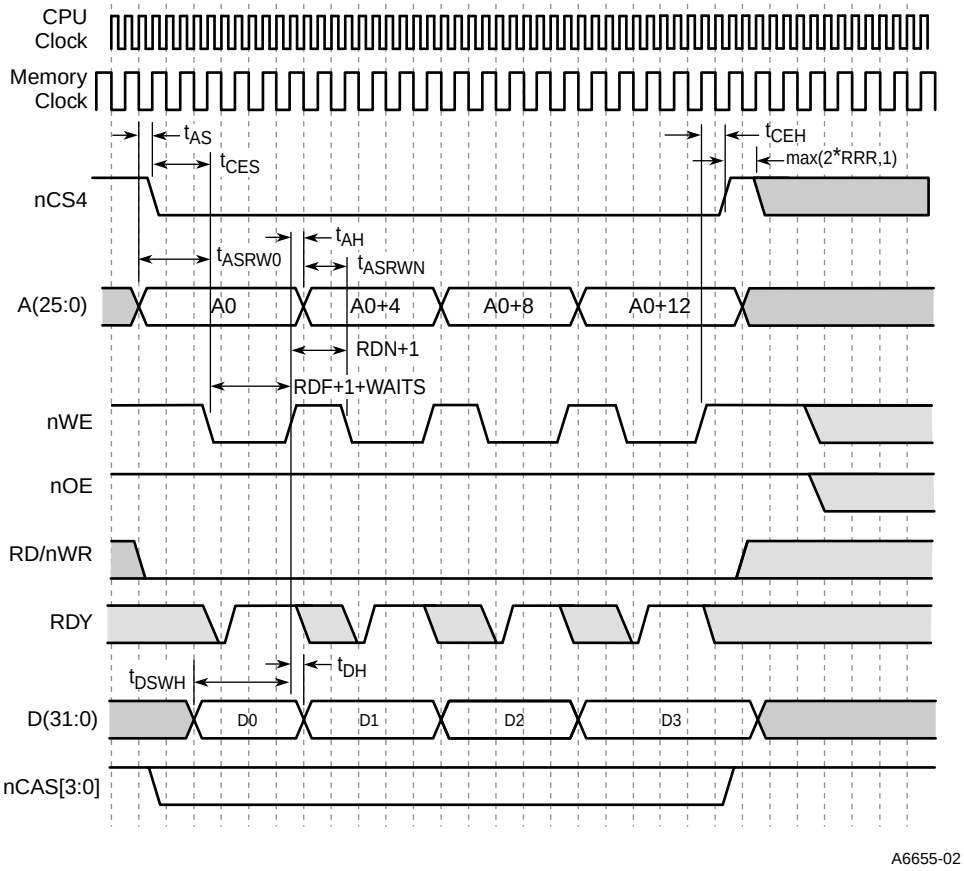


Figure 10-18: Flash Write Timing Diagram (2 Writes)

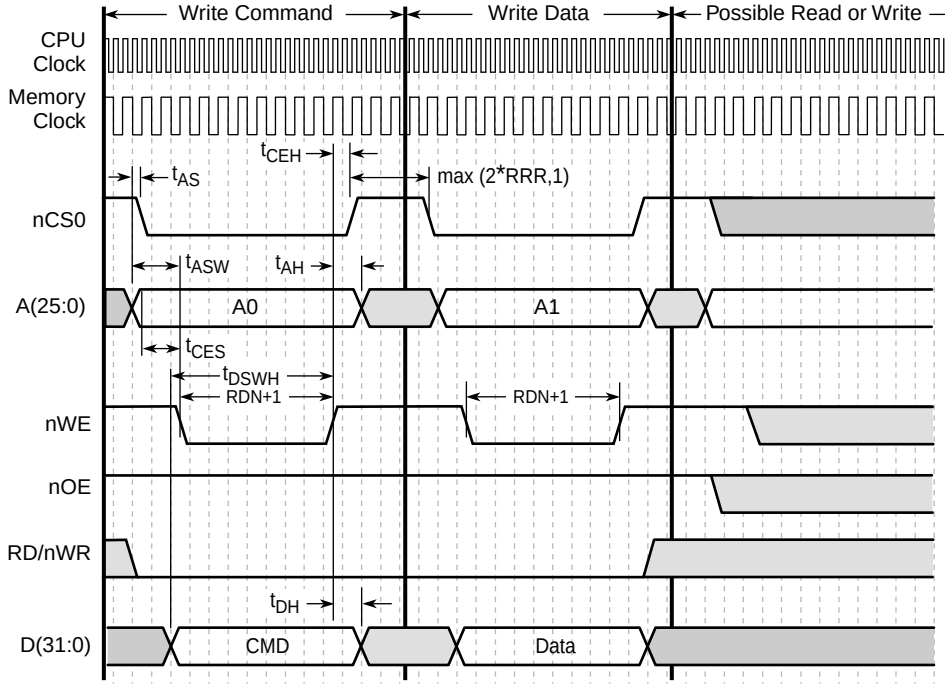
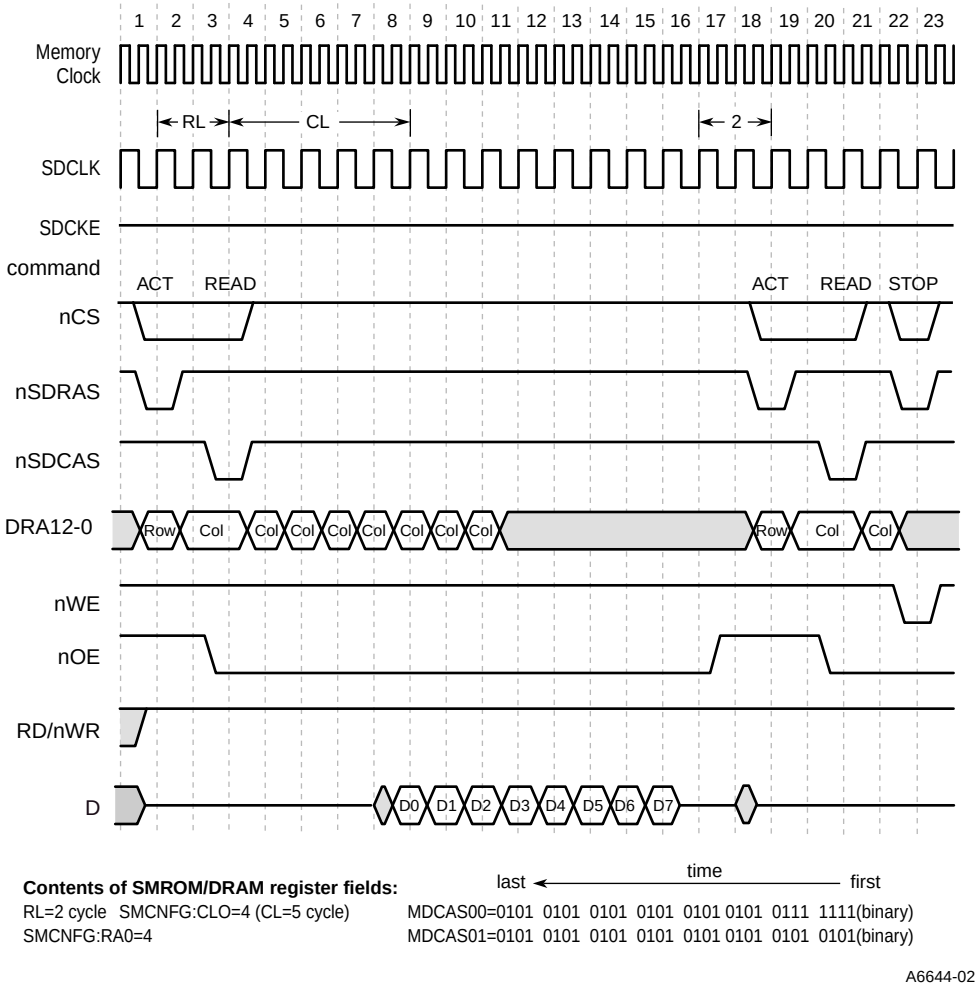


Figure 10-20: SMROM Eight-Beat and Two-Beat Timing for 2 M x 16 Bit Organization (32 Mbit) at Half Memory Clock Frequency (MDREFR:K0DB2=1)



Contents of SMROM/DRAM register fields:

RL=2 cycle SMCNFG:CLO=4 (CL=5 cycle)
SMCNFG:RA0=4

MDCAS00=0101 0101 0101 0101 0101 0101 0111 1111(binary)
MDCAS01=0101 0101 0101 0101 0101 0101 0101 0101(binary)

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Figure 10-24: PCMCIA Memory or I/O 16-Bit Access

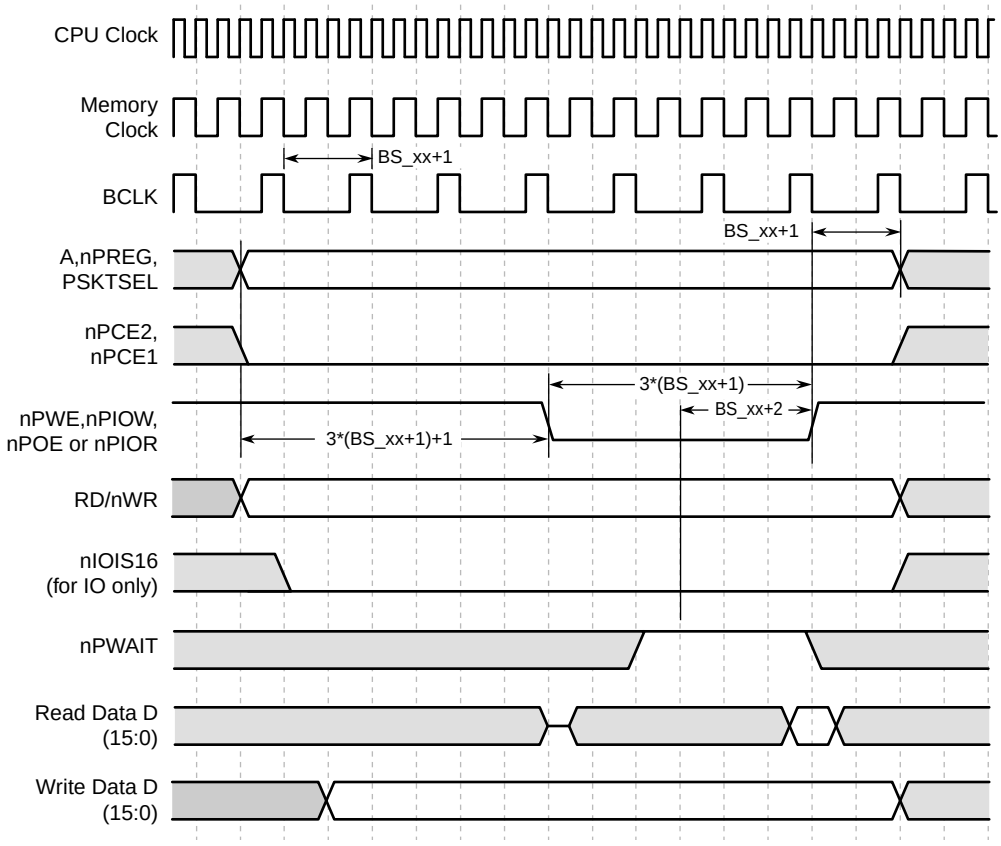
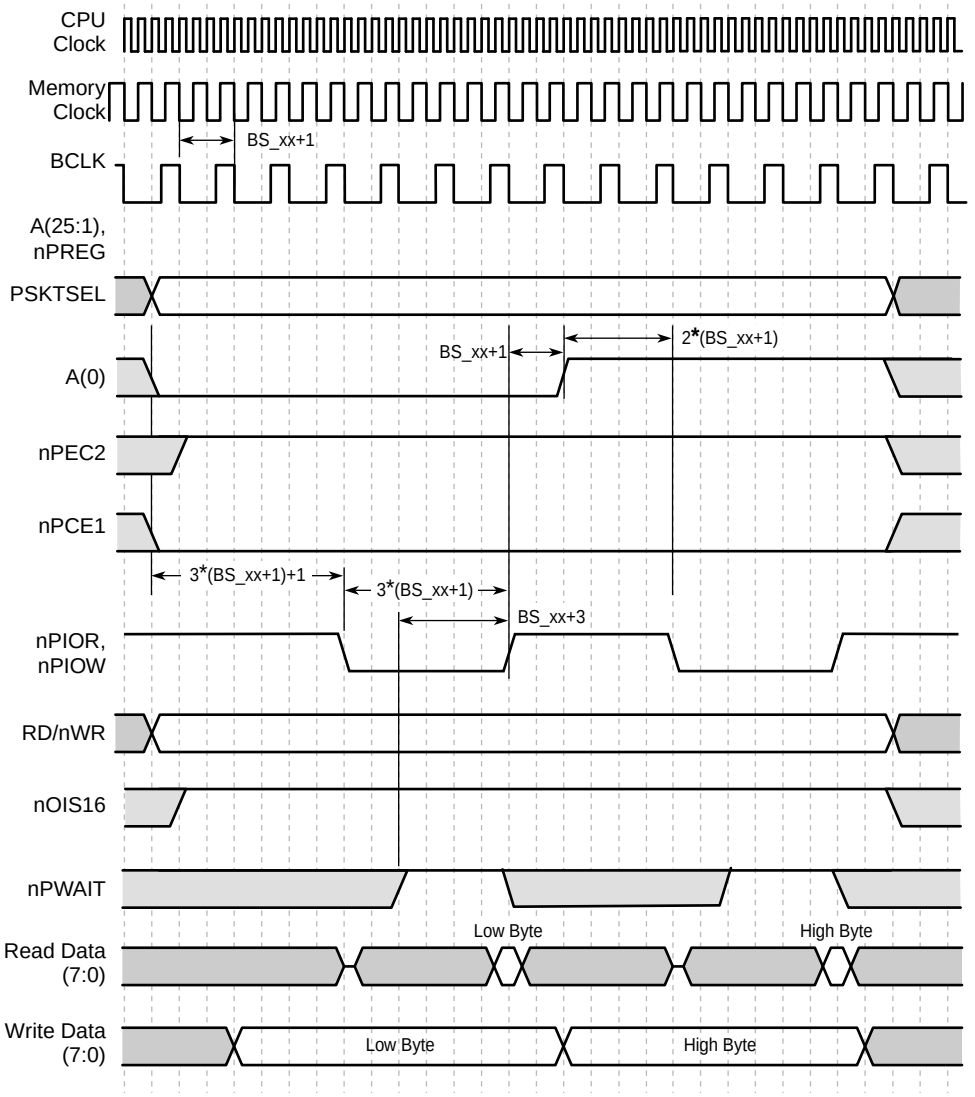


Figure 10-25: PCMCIA I/O 16-Bit Access to 8-Bit Device



13. DRAM Refresh Control Register (MDREFR): Section 10.2.2

Description of bit 31 in the register bit table changed to:

31	SLFRSH	SDRAM self-refresh control/status. It is the control/status bit for entering and exiting SDRAM self-refresh and it is automatically set upon a hardware or sleep reset. SLFRSH can be set by program to force a self-refresh command. E1PIN does not have to be cleared. The appropriate clock run bits (K1RUN and/or K2RUN) must remain set until SDRAM has entered self-refresh and must be set prior to exiting self-refresh (clearing SLFRSH). Also, auto-power-down must be disabled (EAPD=KAPD=0) to ensure power-down-exit upon subsequent clearing of SLFRSH. This capability should be used with extreme caution because the resulting state prohibits automatic transitions for any commands.See Section 10.4.5. Clearing SLFRSH is a part of the hardware or sleep reset procedure for SDRAM. See Section 10.7.1.

14. DRAM/SDRAM Self-Refresh in Sleep Mode: Section 10.4.7

Last sentence in the first paragraph changed to: “SDCLK<2:0> stop running throughout sleep: SDCLK<2:1> are held high; SDCLK<0> is held low if auto-power-down is enabled, or held high if auto-power-down is disabled.”

15. Hardware or Sleep Reset Procedures: Section 10.7.1

Step two changed to the following:

“In systems containing SMROM, write to SMCNFG to configure the CAS latencies (CL fields), row address bit counts (RA fields), and enables (SM bits). A careful software sequence, involving a subsequent write to SMCNFG, is required to change RAS latencies (RL fields): See Section 10.3.1.While any SMROM banks are being configured, all SDRAM banks and SDRAM/SMROM auto-power-down must be disabled.”

16. Alternate Memory Bus Master Mode: Section 10.8

The last three sentences of the first paragraph changed to:

“The RD/nWR pin will remain low. After that the SA-1110 will assert MBGNT (GPIO<21>), the alternate master should start driving all pins (including SDCLK<1>), and the SA-1110 will re-assert SDCKE<1>. The grant sequence and timing are as follows; the Tmem unit of time is the memory clock period (twice the CPU clock period):”

17. Memory Bus Alternate Master: Section 16.8

This section removed because it is redundant with Section 10.8.

18. Test Unit Control Register (TUCR): Section D.1

The description for bit 10 changed to:

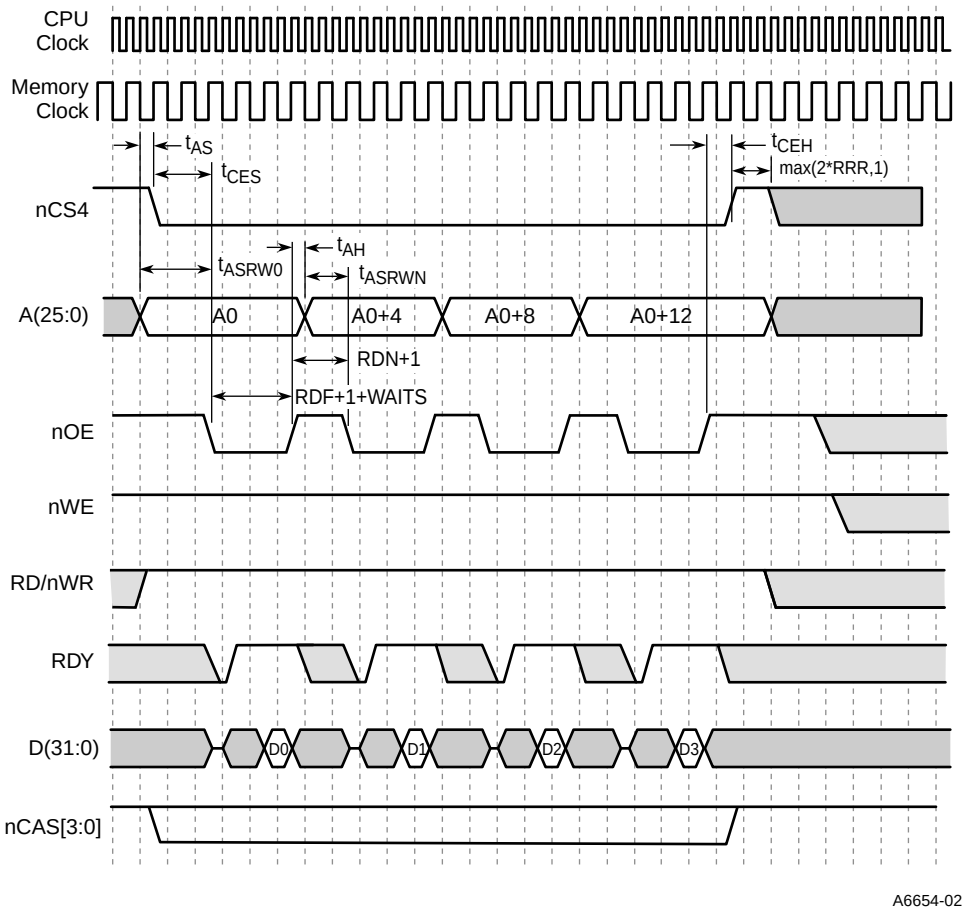
10	MR	Memory request mode. Controls two GPIO pins used for external arbitration and for the memory bus. 0 – GP<21> and GP<22> are not used for an alternate function. 1 – GP<21> and GP<22> are reserved for use as MBGNT and MBREQ, respectively.

19. Power Manager GPIO Sleep State Register (PGSR): Section 9.5.7.7

Section heading changed from “Power Manager GPIO Sleep State Register (PSSR)” to “Power Manager GPIO Sleep State Register (PGSR)”. This section replaced with the following text:

“The GPIO sleep state register (PGSR) allows the user to select the output state of each GPIO pin when the SA-1100 goes into sleep mode. When a transition to sleep is required (either through software or through the assertion of the BATT_FAULT or VDD_FAULT pins), the contents of the PGSR is loaded into the GPIO output data register. [This register is normally controlled by software through the GPSR (set) and GPCR (clear) registers]. Only pins already configured as outputs will reflect the new state; however, all 28 bits of the output register are loaded. After the SA-1100 reenters the run mode from sleep, these GPIO pins retain their programmed sleep state until changed by writing ones to the GPSR or GPCR registers; question marks indicate that the values are unknown at reset. If a pin direction is switched from an input to an output, the last contents of the register will be driven onto the pin.”

20. Variable Latency I/O Read Timing (Burst-of-Four, with One Wait Cycle Per Beat): Figure 10-16



21. ROM Interface Overview: Section 10.5.1

Text changed to: “One memory clock cycle is always added to RDF and RDN. One memory clock cycle is added to RRR if it was set to zero, otherwise it is doubled.”

22. Overview of Operation: Section 10.1

Text changed to: “Two SDRAM/SMROM auto-power-down mode bits (one for clock enables, one for clocks) can be set so that each pin (including SDCKE<1> and SDCLK<2:1>) is automatically deasserted whenever none of the corresponding banks is being accessed.”

23. DRAM Refresh Control Register (MDREFR): Section 10.2.2.

Text changed to: “Auto-power-down, enabled by the KAPD and EAPD bits, is an automatic mechanism for minimizing power consumption in the SA-1110 SDCLK pin drivers and the SDRAM/SMROM devices. EAPD and KAPD must be written to the same value.”

Descriptions of MDREFR:EAPD and MDREFR:KAPD bits changed to:

28	EAPD	SDRAM/SMROM clock enable pin (SDCKE<1:0>) auto-power-down enable. If EAPD=1, each of the clock enable pins (SDCKE<0> for SMROM and SDCKE<1> for SDRAM) will automatically deassert whenever none of the corresponding banks is being accessed. EAPD and KAPD must be written to the same value. See Figure 10-7 and Figure 10-19. Auto-power-down must not be enabled until all other SDRAM/SMROM hardware or sleep reset procedures have been completed. See Section 10.7.1.
29	KAPD	SDRAM/SMROM clock pin (SDCLK<2:0>) auto-power-down enable. If KAPD=1, each of the clock pins (SDCLK<0> for SMROM, SDCLK<1> for SDRAM bank pair 0/1, and SDCLK<2> for SDRAM bank pair 2/3) will automatically deassert (stop running) whenever none of the corresponding banks is being accessed. EAPD and KAPD must be written to the same value. See Figure 10-7 and Figure 10-19. Auto-power-down must not be enabled until all other SDRAM/SMROM hardware or sleep reset procedures have been completed. See Section 10.7.1.

24. Hardware or Sleep Reset Procedures: Section 10.7.1

Added the following step to hardware or sleep reset procedures:

8. In systems containing SDRAM or SMROM, optionally enable auto-power-down by setting MDREFR:EAPD and MDREFR:KAPD.

25. SA-1110 Tool Chains and Operating Systems Table

Removed. See the Intel web site for the latest information about tool chains and operating systems.

26. Pin Operation in Sleep Mode: Section 9.5.6

The following text changed to:

“Type 4 – These pins are I/Os but become inputs during sleep. They can be programmed to hold the pin state at a zero or can be tristated. The receivers on these pins are disabled during sleep. These pins hold their state after sleep mode is exited until either the peripheral_control_hold bit in the PSSR is cleared.”

27. PPC Operation: Section 11.13.1

The following text changed to:

"To keep the same pin direction and state after sleep mode has been negated but before the user reprograms the peripherals, the system control module's power manager maintains the peripherals' pin direction and state following sleep negation until the peripheral control hold bit (PSSR:PH), located in the power manager, is cleared (by writing a one to it). Therefore, the pin direction and state established during sleep using the sleep mode direction register remains intact following the negation of sleep until the PH bit is cleared. Once PH is cleared, control of the peripherals' pins is given back to the individual peripherals and to the PPC unit."

28. PPC Sleep Mode Pin Direction Register: Section 11.13.6

"The power manager contains a control bit called the peripheral control hold (PSSR:PH). This bit is set upon exit from sleep mode and indicates that the peripheral pins are being held in their sleep state. manager Following sleep, the user should first reprogram the peripherals and the PPC, then clear PH (by writing a one to it) in order to give control of the pins back to the peripheral units."

29. Variable Latency I/O Interface Overview: Section 10.5.5

The first sentence of the second paragraph changed to:

"Both reads and writes differ from SRAM in that the SA-1110 starts sampling the data ready input (RDY) at RDF-1 memory cycles after assertion of nOE or nWE: two (2) memory cycles prior to end of minimum nOE or nWE assertion."

30. Software Dcache Flush: Section 6.2.3

The following code example changed from "movr0, 0hE000000" to "movr0, 0hE0000000".

31. Sleep Mode: Section 9.5.3

Last sentence changed to: " Status bits in the reset controller status register (RCSR) may be read to indicate to software that the reset was due to sleep mode."

32. SA-1110 AC Timing Table - Memory Bus: Table 13-2.

The following output signals added to Table 13-2:

Pin Name	Symbol	Parameter	Min	Max	Unit	Note
SDCK<1:0>,SDCLK<2:0>, nCS<3:0>, nRAS/nSDCS<3:0>, A<25:10>, D<31:0>; nSDRAS, nSDCAS, nWE, nCAS/DQM<3:0>		Output pin transition times between 0.4V and 2.4V	0.8	2.5	ns	
All other output signals		Output pin transition times between 0.4V and 2.4V	1.6	4.5	ns	

33. UDC Register Definitions: Section 11.8.2

The last sentence of the Note to Section 11.8.2. changed from: " For example, when clearing a bit, read it back until the bit is actually cleared before going on." to "For example, when writing a UDC register followed by an immediate read to verify data in the same register, the first read will be invalid and the second read will have correct data."

34. Valid Settings for the DDARn Register: Table 11-6

Settings for serial port 2 and serial port 4 in Table 11-6 changed to:

Unit Name	Function	Device Address	DDAR Fields					
			DA<31:8>	DS<3:0>	DW	BS	E	RW
Serial port 0	UDC transmit	0x 8000 0028	0x80000A	0000	0	1	0/1	0
	UDC receive	0x 8000 0028	0x80000A	0001	0	1	0/1	1
Serial port 1	SDLC transmit	0x 8002 0078	0x80801E	0010	0	0	0/1	0
	SDLC receive	0x 8002 0078	0x80801E	0011	0	0	0/1	1
	UART transmit	0x 8001 0014	0x804005	0100	0	0	0/1	0
	UART receive	0x 8001 0014	0x804005	0101	0	0	0/1	1
Serial port 2	HSSP transmit	0x 8004 006C	0x81001B	0110	0	1	0/1	0
	HSSP receive	0x 8004 006C	0x81001B	0111	0	1	0/1	1
	UART transmit	0x 8003 0014	0x80C005	0110	0	0	0/1	0
	UART receive	0x 8003 0014	0x80C005	0111	0	0	0/1	1
Serial port 3	UART transmit	0x 8005 0014	0x814005	1000	0	0	0/1	0
	UART receive	0x 8005 0014	0x814005	1001	0	0	0/1	1
Serial port 4	MCP transmit (audio)	0x 8006 0008	0x818002	1010	1	1	0/1	0
	MCP receive (audio)	0x 8006 0008	0x818002	1010	1	1	0/1	1
	MCP transmit (telecom)	0x 8006 000C	0x818003	1100	1	1	0/1	0
	MCP receive (telecom)	0x 8006 000C	0x818003	1101	1	1	0/1	1
	SSP transmit	0x 8007 006C	0x81C01B	1110	1	1	0/1	0
	SSP receive	0x 8007 006C	0x81C01B	1111	1	1	0/1	1

35. GPIO Alternate Functions Table: Section 9.1.2

Added the following footnote to the GPIO Alternate Functions Table in Section 9.1.2:

†To enable RCLK_OUT, it is also necessary to set bits 31:29 of the Test Unit Control Register (TUCR) = 0b100. See Appendix D for more information about the TUCR.

36. Intel® StrongARM®SA-1110 Boundary-Scan (BS) Register: Section 16.6.3

Added the following text as a new paragraph between paragraphs 4 and 5 of section 16.6.3.

"Table 12-4 shows the correspondence between boundary-scan cells and system pins, system direction controls, and system output enables. The cells are listed in the order in which they are connected in the boundary-scan register, starting with the cell closest to TDI."

37. Boundary-Scan Signals and Pins: Table 16-2

Added the following boundary-scan signals and pins table.

Table 12-4 shows the SA-1110 correspondence between boundary-scan cells and system pins, system direction controls and system output enables.

Key to Table:

IN	Input pad
OUT	Output pad
EN	Enable
OEL	Output enable latch
OEL†	Output enable latch for nWE, nOE, nSDRAS, nSDCAS, nRAS 0, nCAS 3:0, A 25:0
ICL	Input capture latch
OCL	Output capture latch
VDCL	Voltage differential capture latch

Table 12-4. Boundary-Scan Signals and Pins (Sheet 1 of 4)

No.	Pin	Type	BS Cell	BS Function	Guard Value EX		No.	Pin	Type	BS Cell	BS Function	Guard Value EX	
from TDI													
1	BATT_FAULT	IN	qjti	ICL			35	D 10	IN	qjti	ICL		
2	VDD_FAULT	IN	qjti	ICL			36	D 18	OUT	qjto	OCL		
3	PWR_EN	OUT	qjtogp	OCL			37	D 18	IN	qjti	ICL		
4	SFRM_C	EN	qjtena	OEL			38	D 26	OUT	qjto	OCL		
5	SFRM_C	OUT	qjto	OCL			39	D 26	IN	qjti	ICL		
6	SFRM_C	IN	qjti	ICL			40	D 3	OUT	qjto	OCL		
7	SCLK_C	EN	qjtena	OEL			41	D 3	IN	qjti	ICL		
8	SCLK_C	OUT	qjto	OCL			42	D 11	OUT	qjto	OCL		
9	SCLK_C	IN	qjti	ICL			43	D 11	IN	qjti	ICL		
10	RXD_C	EN	qjtena	OEL			44	D 19	OUT	qjto	OCL		
11	RXD_C	OUT	qjto	OCL			45	D 19	IN	qjti	ICL		
12	RXD_C	IN	qjti	ICL			46	D 27	OUT	qjto	OCL		
13	TXD_C	EN	qjtena	OEL			46	D 27	IN	qjti	ICL		
14	TXD_C	OUT	qjto	OCL			48	D 4	OUT	qjto	OCL		
15	TXD_C	IN	qjti	ICL			49	D 4	IN	qjti	ICL		
16	D 0	OUT	qjto	OCL			50	D 12	OUT	qjto	OCL		
17	D 0	IN	qjti	ICL			51	D 12	IN	qjti	ICL		
18	D 8	OUT	qjto	OCL			52	D 20	OUT	qjto	OCL		
19	D 8	IN	qjti	ICL			53	D 20	IN	qjti	ICL		
20	D 16	OUT	qjto	OCL			54	D 28	OUT	qjto	OCL		
21	D 16	IN	qjti	ICL			55	D 28	IN	qjti	ICL		
22	D 24	OUT	qjto	OCL			56	D 5	OUT	qjto	OCL		
23	D 24	IN	qjti	ICL			57	D 5	IN	qjti	ICL		
24	D 1	OUT	qjto	OCL			58	D 13	OUT	qjto	OCL		
25	D 1	IN	qjti	ICL			59	D 13	IN	qjti	ICL		
26	D 9	OUT	qjto	OCL			60	D 21	OUT	qjto	OCL		
27	D 9	IN	qjti	ICL			61	D 21	IN	qjti	ICL		
28	D 17	OUT	qjto	OCL			62	D 29	OUT	qjto	OCL		
29	D 17	IN	qjti	ICL			63	D 29	IN	qjti	ICL		
30	D 25	OUT	qjto	OCL			64	D 6	OUT	qjto	OCL		
31	D 25	IN	qjti	ICL			65	D 6	IN	qjti	ICL		
32	D 2	OUT	qjto	OCL			66	D 14	OUT	qjto	OCL		
33	D 2	IN	qjti	ICL			67	D 14	IN	qjti	ICL		
34	D 10	OUT	qjto	OCL			68	D 22	OUT	qjto	OCL		

Table 12-4. Boundary-Scan Signals and Pins (Sheet 2 of 4)

No.	Pin	Type	BS Cell	BS Function	Guard Value EX		No.	Pin	Type	BS Cell	BS Function	Guard Value EX	
69	D 22	IN	qjti	ICL			122	GP 16	OUT	qjtogp	OCL		
70	D 30	OUT	qjto	OCL			123	GP 16	IN	qjti	ICL		
71	D 30	IN	qjti	ICL			124	GP 15	EN	qjtenap	OEL		
72	D 7	OUT	qjto	OCL			125	GP 15	OUT	qjtogp	OCL		
73	D 7	IN	qjti	ICL			126	GP 15	IN	qjti	ICL		
74	D 15	OUT	qjto	OCL			127	GP 14	EN	qjtenap	OEL		
75	D 15	IN	qjti	ICL			128	GP 14	OUT	qjtogp	OCL		
76	D 23	OUT	qjto	OCL			129	GP 14	IN	qjti	ICL		
77	D 23	IN	qjti	ICL			130	GP 13	EN	qjtenap	OEL		
78	D 31	OUT	qjto	OCL			131	GP 13	OUT	qjtogp	OCL		
79	D 31	IN	qjti	ICL			132	GP 13	IN	qjti	ICL		
80	D 31:0	EN	qjtena	OEL			133	GP 12	EN	qjtenap	OEL		
81	SDCLK 2	OUT	qjto	D 31:0 OEL			134	GP 12	OUT	qjtogp	OCL		
82	SDCKE 1	OUT	qjto	OCL			135	GP 12	IN	qjti	ICL		
83	SDCLK 1	EN	qjto	OEL			136	GP 11	EN	qjtenap	OEL		
84	SDCKE 1	OUT	qjto	OCL			137	GP 11	OUT	qjtogp	OCL		
85	SDCLK 0	OUT	qjto	OCL			138	GP 11	IN	qjti	ICL		
86	SDCKE 0	OUT	qjto	OCL			139	GP 10	EN	qjtenap	OEL		
87	SMROM_EN	IN	qjti	ICL			140	GP 10	OUT	qjtogp	OCL		
88	GP 27	EN	qjtenap	OEL			141	GP 10	IN	qjti	ICL		
89	GP 27	OUT	qjtogp	OCL			142	GP 9	EN	qjtenap	OEL		
90	GP 27	IN	qjti	ICL			143	GP 9	OUT	qjtogp	OCL		
91	GP 26	EN	qjtenap	OEL			144	GP 9	IN	qjti	ICL		
92	GP 26	OUT	qjtogp	OCL			145	GP 8	EN	qjtenap	OEL		
93	GP 26	IN	qjti	ICL			146	GP 8	OUT	qjtogp	OCL		
94	GP 25	EN	qjtenap	OEL			147	GP 8	IN	qjti	ICL		
95	GP 25	OUT	qjtogp	OCL			148	GP 7	EN	qjtenap	OEL		
96	GP 25	IN	qjti	ICL			149	GP 7	OUT	qjtogp	OCL		
97	GP 24	EN	qjtenap	OEL			150	GP 7	IN	qjti	ICL		
98	GP 24	OUT	qjtogp	OCL			151	GP 6	EN	qjtenap	OEL		
99	GP 24	IN	qjti	ICL			152	GP 6	OUT	qjtogp	OCL		
100	GP 23	EN	qjtenap	OEL			153	GP 6	IN	qjti	ICL		
101	GP 23	OUT	qjtogp	OCL			154	GP 5	EN	qjtenap	OEL		
102	GP 23	IN	qjti	ICL			155	GP 5	OUT	qjtogp	OCL		
103	GP 22	EN	qjtenap	OEL			156	GP 5	IN	qjti	ICL		
104	GP 22	OUT	qjtogp	OCL			157	GP 4	EN	qjtenap	OEL		
105	GP 22	IN	qjti	ICL			158	GP 4	OUT	qjtogp	OCL		
106	GP 21	EN	qjtenap	OEL			159	GP 4	IN	qjti	ICL		
107	GP 21	OUT	qjtogp	OCL			160	GP 3	EN	qjtenap	OEL		
108	GP 21	IN	qjti	ICL			161	GP 3	OUT	qjtogp	OCL		
109	GP 20	EN	qjtenap	OEL			162	GP 3	IN	qjti	ICL		
110	GP 20	OUT	qjtogp	OCL			163	GP 2	EN	qjtenap	OEL		
111	GP 20	IN	qjti	ICL			164	GP 2	OUT	qjtogp	OCL		
112	GP 19	EN	qjtenap	OEL			165	GP 2	IN	qjti	ICL		
113	GP 19	OUT	qjtogp	OCL			166	GP 1	EN	qjtenap	OEL		
114	GP 19	IN	qjti	ICL			167	GP 1	OUT	qjtogp	OCL		
115	GP 18	EN	qjtenap	OEL			168	GP 1	IN	qjti	ICL		
116	GP 18	OUT	qjtogp	OCL			169	GP 0	EN	qjtenap	OEL		
117	GP 18	IN	qjti	ICL			170	GP 0	OUT	qjtogp	OCL		
118	GP 17	EN	qjtenap	OEL			171	GP 0	IN	qjti	ICL		
119	GP 17	OUT	qjtogp	OCL			172	L_BIAS	EN	qjtena	OEL		
120	GP 17	IN	qjti	ICL			173	L_BIAS	OUT	qjto	OCL		
121	GP 16	EN	qjtenap	OEL			174	L_BIAS	IN	qjti	ICL		

Table 12-4. Boundary-Scan Signals and Pins (Sheet 3 of 4)

No.	Pin	Type	BS Cell	BS Function	Guard Value EX		No.	Pin	Type	BS Cell	BS Function	Guard Value EX	
175	L_PCLK	EN	qjtena	OEL			228	nCAS 2	OUT	qjto	OCL		
176	L_PCLK	OUT	qjto	OCL			229	nCAS 1	OUT	qjto	OCL		
177	L_PCLK	IN	qjti	ICL			230	nCAS 0	OUT	qjto	OCL		
178	L_DD 0	EN	qjtena	OEL			231	RD/nWR	OUT	qjto	OCL		
179	L_DD 0	OUT	qjto	OCL			232	RDY	IN	qjti	ICL		
180	L_DD 0	IN	qjti	ICL			233	nCS 5	OUT	qjto	OCL		
181	L_DD 1	EN	qjtena	OEL			234	nCS 4	OUT	qjto	OCL		
182	L_DD 1	OUT	qjto	OCL			235	nCS 3	OUT	qjto	OCL		
183	L_DD 1	IN	qjti	ICL			236	nCS 2	OUT	qjto	OCL		
184	L_DD 2	EN	qjtena	OEL			237	nCS 1	OUT	qjto	OCL		
185	L_DD 2	OUT	qjto	OCL			238	nCS 0	OUT	qjto	OCL		
186	L_DD 2	IN	qjti	ICL			239	A 25	OUT	qjto_fast	OCL		
187	L_DD 3	EN	qjtena	OEL			240	A 24	OUT	qjto_fast	OCL		
188	L_DD 3	OUT	qjto	OCL			241	A 23	OUT	qjto_fast	ICL		
189	L_DD 3	IN	qjti	ICL			242	A 22	OUT	qjto_fast	OCL		
190	L_DD 4	EN	qjtena	OEL			243	A 21	OUT	qjto_fast	OCL		
191	L_DD 4	OUT	qjto	OCL			244	A 20	OUT	qjto_fast	OCL		
192	L_DD 4	IN	qjti	ICL			245	A 19	OUT	qjto_fast	OCL		
193	L_DD 5	EN	qjtena	OEL			246	A 18	OUT	qjto_fast	OCL		
194	L_DD 5	OUT	qjto	OCL			247	A 17	OUT	qjto_fast	OCL		
195	L_DD 5	IN	qjti	ICL			248	A 16	OUT	qjto_fast	OCL		
196	L_DD 6	EN	qjtena	OEL			249	A 15	OUT	qjto_fast	OCL		
197	L_DD 6	OUT	qjto	OCL			250	A 14	OUT	qjto_fast	ICL		
198	L_DD 6	IN	qjti	ICL			251	A 13	OUT	qjto_fast	OCL		
199	L_DD 7	EN	qjtena	OEL			252	A 12	OUT	qjto_fast	OCL		
200	L_DD 7	OUT	qjto	OCL			253	A 11	OUT	qjto_fast	OCL		
201	L_DD 7	IN	qjti	ICL			254	A 10	OUT	qjto_fast	OCL		
202	L_LCLK	EN	qjtena	OEL			255	A 9	OUT	qjto	OCL		
203	L_LCLK	OUT	qjto	OCL			256	A 8	OUT	qjto	OCL		
204	L_LCLK	IN	qjti	ICL			257	A 7	OUT	qjto	OCL		
205	L_FCLK	EN	qjtena	OEL			258	A 6	OUT	qjto	OCL		
206	L_FCLK	OUT	qjto	OCL			259	A 5	OUT	qjto	ICL		
207	L_FCLK	IN	qjti	ICL			260	A 4	OUT	qjto	OCL		
208	nPOE	OUT	qjto	OCL			261	A 3	OUT	qjto	OCL		
209	nPWE	OUT	qjto	OCL			262	A 2	OUT	qjto	OCL		
210	nPIOR	OUT	qjto	OCL			263	A 1	OUT	qjto	OCL		
211	nPIOW	OUT	qjto	OCL			264	A 0	OUT	qjto	OCL		
212	PSKTSEL	OUT	qjto	OCL			265	UDC-	EN	qjtena	OEL		
213	nIOIS16	IN	qjti	ICL			266	UDC-	OUT	qjto	OCL		
214	nPWAIT	IN	qjti	ICL			267	UDC-	IN	qjti	ICL		
215	nPREG	OUT	qjto	OCL			268	UDC-/UDC+	IN	qjti	UDC-/UDC+ VDCL		
216	nPCE 2	OUT	qjto	OCL			269	UDC+	EN	qjtena	OEL		
217	nPCE 1	OUT	qjto	OCL			270	UDC+	OUT	qjto	OCL		
218	—	EN	qjtena	OEL†			271	UDC+	IN	qjti	ICL		
219	nWE	OUT	qjto	OCL			272	RXD_1	EN	qjtena	OEL		
220	nOE	OUT	qjto	OCL			273	RXD_1	OUT	qjto	OCL		
221	nSDRAS	OUT	qjto	OCL			274	RXD_1	IN	qjti	ICL		
222	nSDCAS	OUT	qjto	OCL			275	TXD_1	EN	qjtena	OEL		
223	nRAS 3	OUT	qjto	OCL			276	TXD_1	OUT	qjto	OCL		
224	nRAS 2	OUT	qjto	OCL			277	TXD_1	IN	qjti	ICL		
225	nRAS 1	OUT	qjto	OCL			278	RXD_2	EN	qjtena	OEL		
226	nRAS 0	OUT	qjto	OCL			279	RXD_2	OUT	qjto	OCL		
227	nCAS 3	OUT	qjto	OCL			280	RXD_2	IN	qjti	ICL		

Table 12-4. Boundary-Scan Signals and Pins (Sheet 4 of 4)

No.	Pin	Type	BS Cell	BS Function	Guard Value EX		No.	Pin	Type	BS Cell	BS Function	Guard Value EX	
281	TXD_2	EN	qjtena	OEL			287	TXD_3	EN	qjtena	OEL		
282	TXD_2	OUT	qjto	OCL			288	TXD_3	OUT	qjto	OCL		
283	TXD_2	IN	qjti	ICL			289	TXD_3	IN	qjti	ICL		
284	RXD_3	EN	qjtena	OEL			290	nRESET	IN	qjti	ICL		
285	RXD_3	OUT	qjto	OCL			291	nRESET_OUT	OUT	qjto	OCL		
286	RXD_3	IN	qjti	ICL			292	ROM_SEL	IN	qjti	ICL		
								to TDO					

NOTES:
1. The Boundary Scan (BS) numbers are listed in order from the first BS latch after the TDI input pin. Thus, for a given BS pattern, the first bit input will land in the 292nd BS latch and the last bit will land in the first BS latch.
2. BS latch 80 controls the tristate enable of the D 31:0 pins. A “1” in latch 80 will tristate the D 31:0 pins.
3. BS latch 83 controls the tristate enable for output pin SDCLK 1. A “1” in latch 83 will tristate SDCLK 1.
4. BS latch 218 controls the tristate enable of nWE, nOE, nSDRAS, nSDCAS, nRAS 0, nCAS 3:0, and A 25:0. A “1” in latch 218 will tristate these pins.
5. The output enable latches for UDC- and UDC+, 265 and 269, will tristate the outputs when a “1” is latched in.
6. For all other output or in/out pins, a “0” in the output enable latch will tristate the output in.

38. GPIO Alternate Functions: Section 9.1.2

In the table showing each GPIO pin and its corresponding alternate function, changed the signal description for GPIO pin 25 from “Trimmed 1-Hz clock” to “Real time clock”.

39. UART Data Register: Section 11.11.6

Added the following note to the end of section 11.11.6:

Note: There may be a delay between the writing of data in the transit FIFO and the assertion of TBY in UTSR1. When the TBY status bit is set, there is some propagation delay for data moving through the FIFO and getting to the serial shifter. The programmer should either use the interrupt functionality of the UART module or wait for a 0 to 1 transition and then a 1 to 0 transition of TBY to ensure that the data is transmitted.

40. Reset Controller Status Register: Section 9.6.1.2

Deleted “Note” to description of RCSR register bit 3.

41. Reset Interrupt Mask: Section 11.8.3.8

Revised description of UDCCR register bit 0 as follows:

Bit	Name	Description
0	UDD	UDD disable. 0 – UDD enabled, UDC+ and UDC- used for USB serial transmission/reception. 1 – UDD disabled.

42. Address Field: Section 11.10.2.3

Section 11.10.2.3. replaced with the following text:

"The 8-bit address field is used by a transmitter to target a select group of receivers when multiple stations are connected to the same set of serial lines. The address allows up to 255 stations to be uniquely addressed (00000000 to 11111110). The global address (11111111) is used to broadcast messages to all stations. Register HSCR1 is used to program a unique address for broadcast recognition. Control bit HSCR0:AME is used to enable/disable the address match function. Note that the address of received frames is stored in the receive FIFO along with normal data and that it is transmitted and received starting with its LSB and ending with its MSB."

43. Pin State During Sleep: Table 9-3

Corrected typo in title from "Pin State During Step" to "Pin State During Sleep".

44. Alternate Memory Bus Master Mode: Section 10.8

Change sentence from "All other memory and PCMCIA pins remain driven." to "All other memory and PCMCIA pin remain driven, including SDCLK 2 is driven to 0, SDCLK 0 is driven to 0, and SDCKE 0 is driven to 1."

45. Exiting Idle Mode: Section 9.5.2.2

Added the following sentence to the end of first paragraph: "Note that the user should re-enable clock switching."

46. Module Considerations: Section 13.2

Title changed to "Model Considerations".

47. Register 0 – ID: Section 5.2.1

Changed the ID code and added the following stepping information:

Register 0 – ID **Read-Only**

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
69	Architecture Version	Part Number	Stepping

Architecture Version	ARM® architecture version 01 = Version 4
Part Number	Part number B11 = SA1110
Stepping	Stepping revision of SA-1110 0000 = A0 stepping 0100 = B0 stepping 0101 = B1 stepping

48. SA-1110 AC Timing Table - Memory Bus: Table 13-2

Output signal SDCKE 1:0 corrected and output signal nOE added to Table 13-2 as follows:

Pin Name	Symbol	Parameter	Min.	Max	Unit	Note
SDCKE 1:0,SDCLK 2:0, nCS 3:0, nRAS/nSDCS 3:0, A 25:10, D 31:0; nSDRAS, nSDCAS, nWE, nCAS/DQM 3:0; nOE		Output pin transition times between 0.4V and 2.4V	0.8	2.5	ns	
All other output signals		Output pin transition times between 0.4V and 2.4V	1.6	4.5	ns	

49. Aborts and Nonexistent Memory: Section 10.1.7

The second sentence of the third paragraph changed to:

“This technique is used in the hardware and sleep reset procedures (see Section 10.7.1) and the software and watchdog reset procedures (see Section 10.7.1).”

50. DRAM Configuration Register (MDCNFG): Section 10.2.1

The last sentence of the first paragraph changed to:

“Question marks indicate that the values are unknown at hardware or sleep reset.”

The last sentence in the descriptions of MDCNFG:DE1...0 and MDCNFG:DE3...2 changed to:

“These bits are cleared by hardware or sleep reset.”

51. DRAM Refresh Control Register (MDREFR): Section 10.2.2

The last sentence of the first paragraph change to:

“Question marks indicate that the values are unknown at hardware or sleep reset."

Note below the bit field figure changed to:

"Upon hardware or sleep reset, K0RUN and E0PIN are set to the value of the SMROM_EN pin."

Note above the bit field descriptions changed to:

"Upon hardware or sleep reset, K0RUN and E0PIN are set to the value of the SMROM_EN pin."

Last sentence of the first paragraph of the MDREFR:E0PIN (bit16) description changed to:

"It is set upon hardware or sleep reset if static memory bank 0 (boot space) is configured for SMROM (SMROM_EN=1); otherwise it is cleared upon hardware or sleep reset."

Last sentence of the first paragraph of the MDREFR:K0RUN (bit17) description changed to:

"It is set upon hardware or sleep reset if static memory bank 0 (boot space) is configured for SMROM (SMROM_EN=1); otherwise it is cleared upon hardware or sleep reset."

52. CAS Waveform Rotate Registers (MDCAS00, MDCAS01, MDCAS02, MDCAS20, MDCAS21, MDCAS22): Section 10.2.3

Last sentence of the first paragraph changed to:

"Question marks indicate that the values are unknown at hardware or sleep reset."

First sentence of the last paragraph changed to:

"The hardware or sleep reset value for MDCAS00 (shown below) supports SMROM single word reads at one-half the memory clock frequency (MDREFR:K0DB2=1), with a RAS-to-CAS delay of two cycles. If SMROM_EN=1, this value must be maintained to avoid a mismatch in RAS latency between the SA-1110 and boot SMROM following a subsequent hardware or sleep reset."

53. Static Memory Control Registers (MSC2-0): Section 10.2.4

Second paragraph changed to:

“On hardware or sleep reset, the MSC0:<15:0> field is set to 0b 1111 1111 1111 1x00 (binary) where x represents the inverse of the ROM_SEL pin. This forces nCS(0) to the slowest possible nonburst ROM timings. All other fields in MSC0, MSC1, and MSC2 are unaffected by reset; question marks indicate that the values are unknown at hardware or sleep reset.”

First sentence of the MSCx:RBWx description changed to:

"On hardware or sleep reset, the RBW0 field in MSC0 is loaded with the inverse of the ROM_SEL pin."

Second sentence of the second paragraph of the MSCxRBWx description changed to:

"Also, if nCS<0> is configured for SMROM by holding the SMROM_EN pin high during hardware or sleep reset, the ROM_SEL pin must be held low."

54. Expansion Memory (PCMCIA) Configuration Register (MECR): Section 10.2.5

Last sentence of the first paragraph changed to:

"This register is unaffected by reset; question marks indicate that the values are unknown at hardware or sleep reset."

55. SMROM Configuration Register (SMCNFG): Section 10.3

Last sentence of the first paragraph changed to:

"Question marks indicate that the values are unknown at hardware or sleep reset."

Note below the bit field figure changed to:

"Upon hardware or sleep reset, SM0 is set to the value of the SMROM_EN pin."

Note above the bit field descriptions changed to:

"Upon hardware or sleep reset, SM0 is set to the value of the SMROM_EN pin."

Last sentence of the description of SMCNFG:SM1-0 (bits 1:0) changed to:

"SM0 is set upon hardware or sleep reset if the SMROM_EN pin is held high."

Following sentence added to description of SMCNFG:CL0 (bits 14:12):

“Hardware or sleep reset forces CL0=100. If SMROM_EN=1, CL0 must be maintained at this value to avoid a mismatch in CAS latency between the SA-1110 and boot SMROM following a subsequent hardware or sleep reset.”

Following sentence added to description of SMCNFG:RL0 (bit 15):

“Hardware or sleep reset forces RL0=1. If SMROM_EN=1, RL0 must be maintained at this value to avoid a mismatch in RAS latency between the SA-1110 and boot SMROM following a subsequent hardware or sleep reset.”

56. DRAM/SDRAM Refresh: Section 10.4.6

Last two sentences of the first paragraph changed to:

"Hardware or sleep reset clears the refresh counter. Software and watchdog reset do not affect it."

57. ROM Interface Overview: Section 10.5.1

Third to last sentence of the first paragraph changed to:

"Upon hardware or sleep reset, MSC0<15:0> is initialized such that the RDF, RDN and RRR fields are set to their maximum values to accommodate the slowest nonburst ROMs at initial boot, RT is set to be nonburst ROM, and RBW0 is loaded with the value of the inverse of the ROM_SEL pin."

Second to last sentence of the first paragraph changed to:

"The remaining fields in MSC0, MSC1, and MSC2 are not initialized on hardware or sleep reset."

58. SMROM State Machine: Section 10.5.11

Second sentence of the second paragraph changed to:

"Upon hardware or sleep reset, the SA-1110 is compatible with the following SMROM default mode register settings: RAS latency of 2 cycles, CAS latency of 5 cycles, burst length of 4, and sequential burst addressing."

The following paragraph inserted after the second paragraph:

“If the SMROM_EN pin is held high, MDCAS00, SMCNFG:CL0, and SMCNFG:RL0 must maintain their hardware or sleep reset values to avoid mismatches in CAS latency or RAS latency between the SA-1110 and boot SMROM following a subsequent hardware or sleep reset.”

59. Memory Interface Reset and Initialization: Section 10.7

First sentence changed to:

"On hardware or sleep reset, the dynamic memory interface is disabled."

60. Hardware or Sleep Reset Procedures: Section 10.7.1

First sentence changed to:

"Software is responsible for controlling the following procedures when coming out of hardware or sleep reset."

61. Software or Watchdog Reset Procedures: Section 10.7.2

The following new section added:
“Software is responsible for controlling the following procedures when coming out of software or watchdog reset. They must be completed prior to any SDRAM accesses or writes to MDCNFG or MDREFR, to ensure that every SDRAM row is precharged prior to receiving the next bank activate (ACT) or mode register set (MRS) command.

1. Disable all SDRAM banks by clearing MDCNFG:DE3-0, without changing MDCNFG:DTIM2,0.
2. Trigger a precharge all (PALL) command to SDRAM by attempting a nonburst read or write access to any disabled DRAM bank.
3. Re-enable SDRAM banks by setting MDCNFG:DE3-0.”

62. Timing Parameters: Section 13.6

The introductory paragraph to this section changed to:

"Table 13-2 lists the ac timing parameters for the SA-1110 memory bus. Table 13-3 lists the ac timing parameters for the SA-1110 MCP interface and LCD controller. Values in these tables reflect preliminary data, which Intel reserves the right to change at time of full production release. For timing parameters for 1.55-V devices, contact the Intel Massachusetts Customer Technology Center. "

63. FLASH Memory Timing Diagrams and Parameters: Section 10.5.8

Changed one line in the parameters definition list as follows:

“tDSWH = If RT=00, then: Write data setup to nWE high (deasserted) = 1/2 memory cycle + (RDN+1) memory cycles. If RT=1x, then: Write data setup to nWE high (deasserted) = 1/2 memory cycle + (RDF+1) memory cycles”

Added footnote beneath Figure 10-18 as follows:

“If RT=00 then RDN+1. If RT=1x, then RDF+1.”

64. Exiting Idle Mode: Section 9.5.2.2

This section is changed as follows:

“Any enabled interrupt from the system unit or peripheral unit will cause a transition from idle mode back to run mode. The Interrupt Controller Mask Register (ICMR) is ignored during idle mode. This means that an interrupt does not need to be unmasked to bring the SA-1110 out of idle mode. When an interrupt occurs, the CPU clocks are reactivated, the wait-for-interrupt instruction is completed, and run-program flow resumes. If the interrupt bringing the SA-1110 out of idle is masked, program flow resumes in a linear fashion. If the interrupt bringing the SA-1110 out of idle mode is unmasked, program flow resumes as in any other interrupt service routine. You must reenable clock switching for both circumstances.”

65. Register Summary: Appendix A

In the UART Registers (Serial Port 1) section of this table, changed the UTCR2 entry to read as follows:

- Physical Address: 8003 0008
- Symbol: UTCR2
- Register Name: UART control register 2

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