Intel® StrongARM® SA-110 Microprocessor Spurious Reset

Application Note

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Application Note

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1.0 Introduction

This document describes the noise sensitivity in some applications in the StrongARM® SA-110 Microprocessor and its 21285 core logic configuration. This can occur when the data bus enable (DBE) signal from the 21285 simultaneously tristates the data bus while the SA-110 is driving the majority of the data lines high. Depending on the system implementation, this noise sensitivity can result in a spurious reset. This application note recommends a delay circuit that is intended to function at all bus speeds.

The following related documents may be useful:

- *Intel® StrongARM® SA-110 Microprocessor Technical Reference Manual*
- *Intel® 21285 Core Logic for SA-110 Microprocessor Data Sheet*

See the Support, Products, and Documentation section at the end of this document for ordering information.

2.0 Functional Overview

The SA-110 can encounter a spurious reset when deasserting DBE while all 32 data lines are switching high. The SA-110 susceptibility to reset under these conditions greatly diminishes as the number of switching data lines decreases.

The spurious reset condition occurs as follows. When the DBE signal deasserts, the SA-110 drives data to the output buffer through a flop clocked by MCLK and onto the data lines from a low to high state. The SA-110 output driver tristates while the data lines are at transition level resulting in a sufficient amount of system noise to cause the SA-110 to reset (fail). This condition can be avoided when the DBE signal is delayed properly.

3.0 DBE Delay Circuit Recommendations

It is recommended that the DBE delay deassertion must be moved beyond the critical data bus switching point, but it should not delay this deassertion into the next MCLK cycle. The recommended delay circuit is intended to function at all bus speeds.

The delay circuit should consist of the following components:

1. An inverter to invert the FCLK signal.
2. A D-flop (clocking FCLK) and delay the DBE deassertion.
3. An OR gate to minimize the impact on the DBE signal deassertion.

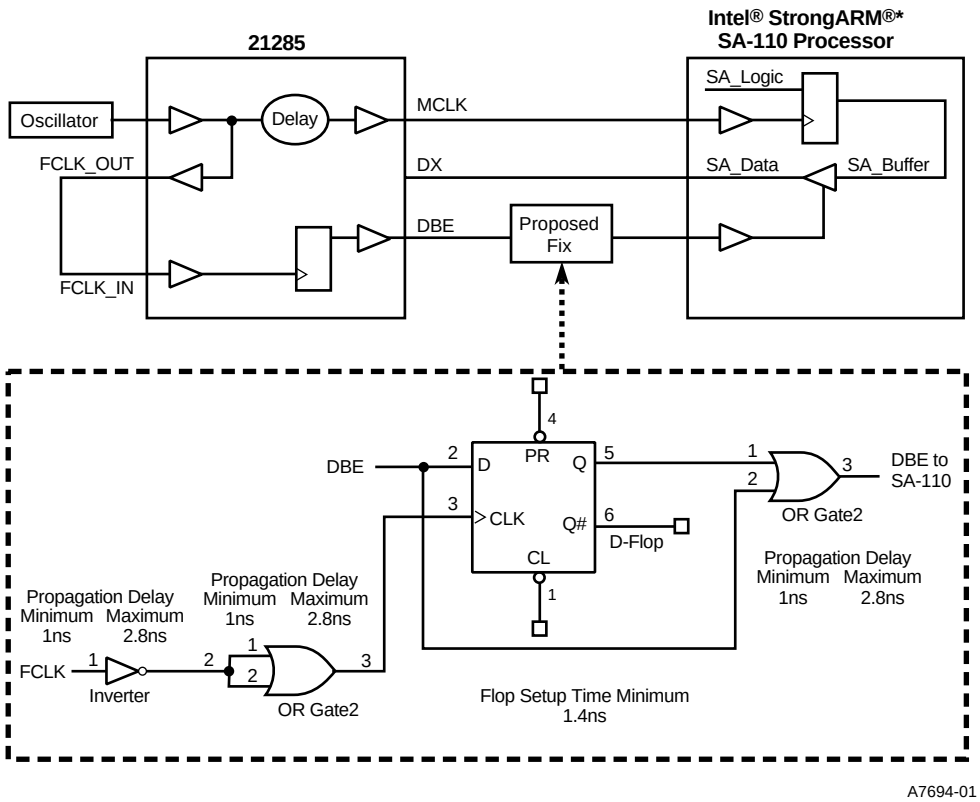
Table 1 lists the recommended devices meeting the specifications for the required delay circuit.

Table 1. Logic Device Specifications

Device	Specification	Minimum	Maximum	Recommendations
Inverter	Propagation Delay	1 ns	2.8 ns	IDT74ALVC1G04* TISN74ALVC04*
OR Gates	Propagation Delay	1 ns	2.8 ns	IDT74ALVC32PG* TISN74ALVC32*
D-flop	Set-up (Ts)	1.4 ns (typical)		Phillips74LVT74PWDHH*
	Propagation Delay	3.0 ns (typical)		

Figure 1 shows a proposed fix for the noise sensitivity between the 21285 and SA-110 system implementation.

Figure 1. Delay Circuit Implementation for the SA-110 and 21285



3.1 Delay Circuit Timing Requirements

Table 2 lists the delay circuit timing requirements.

Table 2. Delay Circuit Timing Specifications

Operation	Specification
Delay for OR gate and inverter	1.0 ns <Tdo < 2.8 ns
CLK to output delay for flop	1.0 ns <Tpo < 3.0 ns
Set-up time (Ts) from data to CLK	Don't care < Ts <1.4 ns
Hold time	0.5 ns < Th

3.2 Set-Up Time Calculation

Table 3 lists the set-up time that must be met to ensure the delay timing requirements .

Table 3. Set-Up Time Calculation

Operation	Specification
Set-up time, worst case	Ts = 1.4 ns
Skew on MCLK and FCLK @ 66 Mhz	Tskew = 0.5 ns
Total time from DBE to CLK	Sum of Ts + Tskew (approximately 1.9 ns to 2.0 ns)

3.3 FCLK Timing

The inverter and buffer (an OR gate can be substituted) provides the inverted function and also delays the FCLK timing for a period between 2.5 ns to 5.6 ns (this includes some wire delay). Therefore, the requirement for DBE deassertion is no later than 8.0 ns (10 ns - 2.0 ns) with respect to FCLK. Table 4 lists the FCLK timing.

Table 4. FCLK Timing

Operation	Specification
FCLK edge, best case	10.0 ns (7.5 ns + 2.5 ns)
FCLK edge, worst case	13.1 ns (7.5 ns + 5.6 ns)

4.0 DBE Deassertion Requirement

The requirement for DBE deassertion, listed in Table 5, is not later than 10.0 ns - 2.0 ns = 8.0 ns with respect to FCLK. These values are within the safe operating area.

Table 5. DBE Deassertion Requirement

Operation	Specification
Earliest DBE deassertion to SA-110	10 + 1.0 + 1.0 = 12.0 ns
Latest DBE deassertion to SA-110	13.1 ns + 2.8 ns + 3.0 ns = 18.9 ns

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